Fig.1

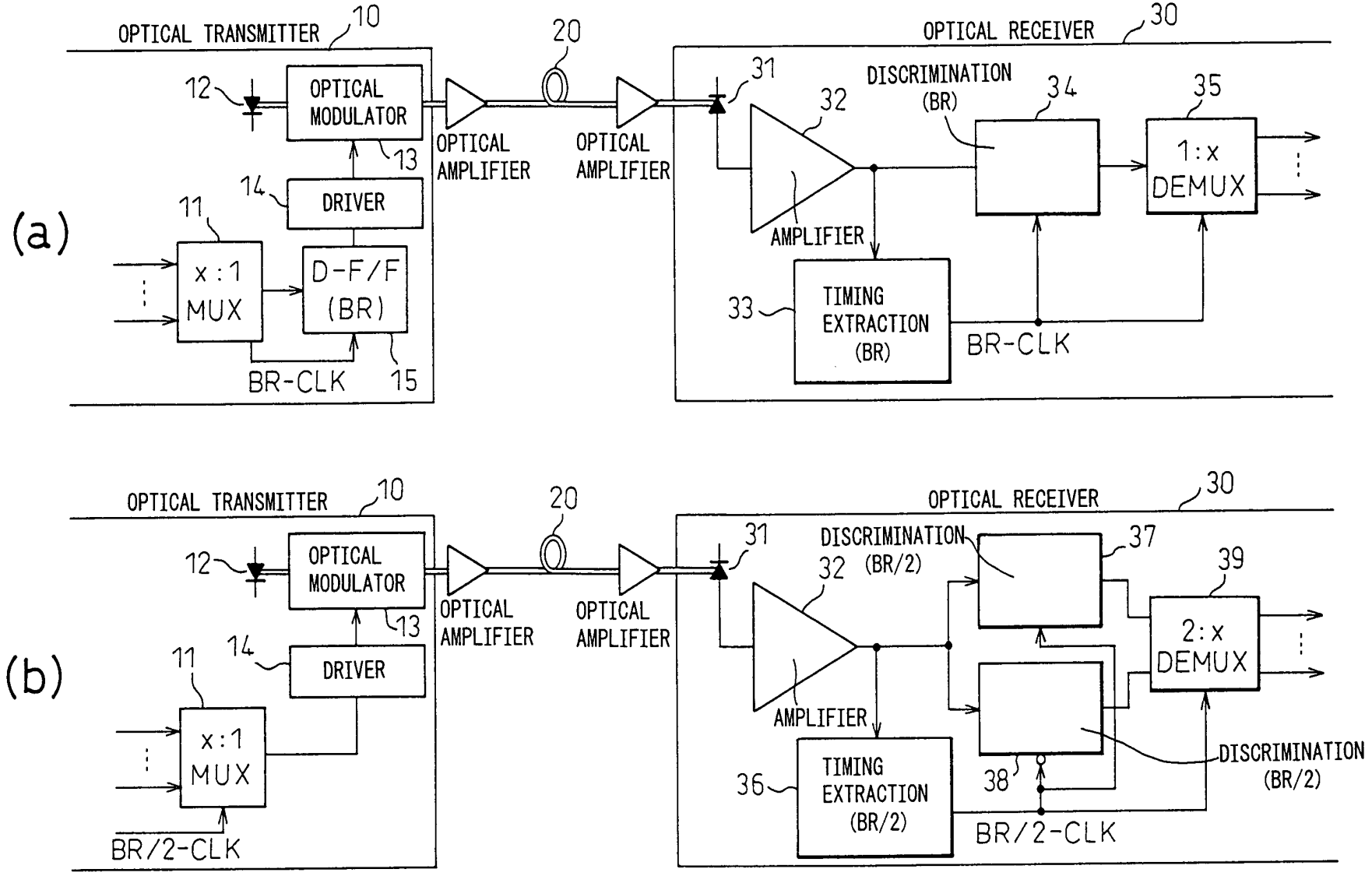

(a)
OPTICAL TRANSMITTER
10
12
OPTICAL MODULATOR
13
14
DRIVER
11
x:1 MUX
D-F/F (BR)
BR-CLK
15
20
OPTICAL AMPLIFIER
OPTICAL AMPLIFIER
OPTICAL RECEIVER
30
31
32
AMPLIFIER
DISCRIMINATION (BR)
34
35
1:x DEMUX
33
TIMING EXTRACTION (BR)
BR-CLK
(b)
OPTICAL TRANSMITTER
10
12
OPTICAL MODULATOR
13
14
DRIVER
11
x:1 MUX
BR/2-CLK
20
OPTICAL AMPLIFIER
OPTICAL AMPLIFIER
OPTICAL RECEIVER
30
31
32
AMPLIFIER
DISCRIMINATION (BR/2)
37
39
2:x DEMUX
36
TIMING EXTRACTION (BR/2)
38
BR/2-CLK
DISCRIMINATION (BR/2)

Fig. 2

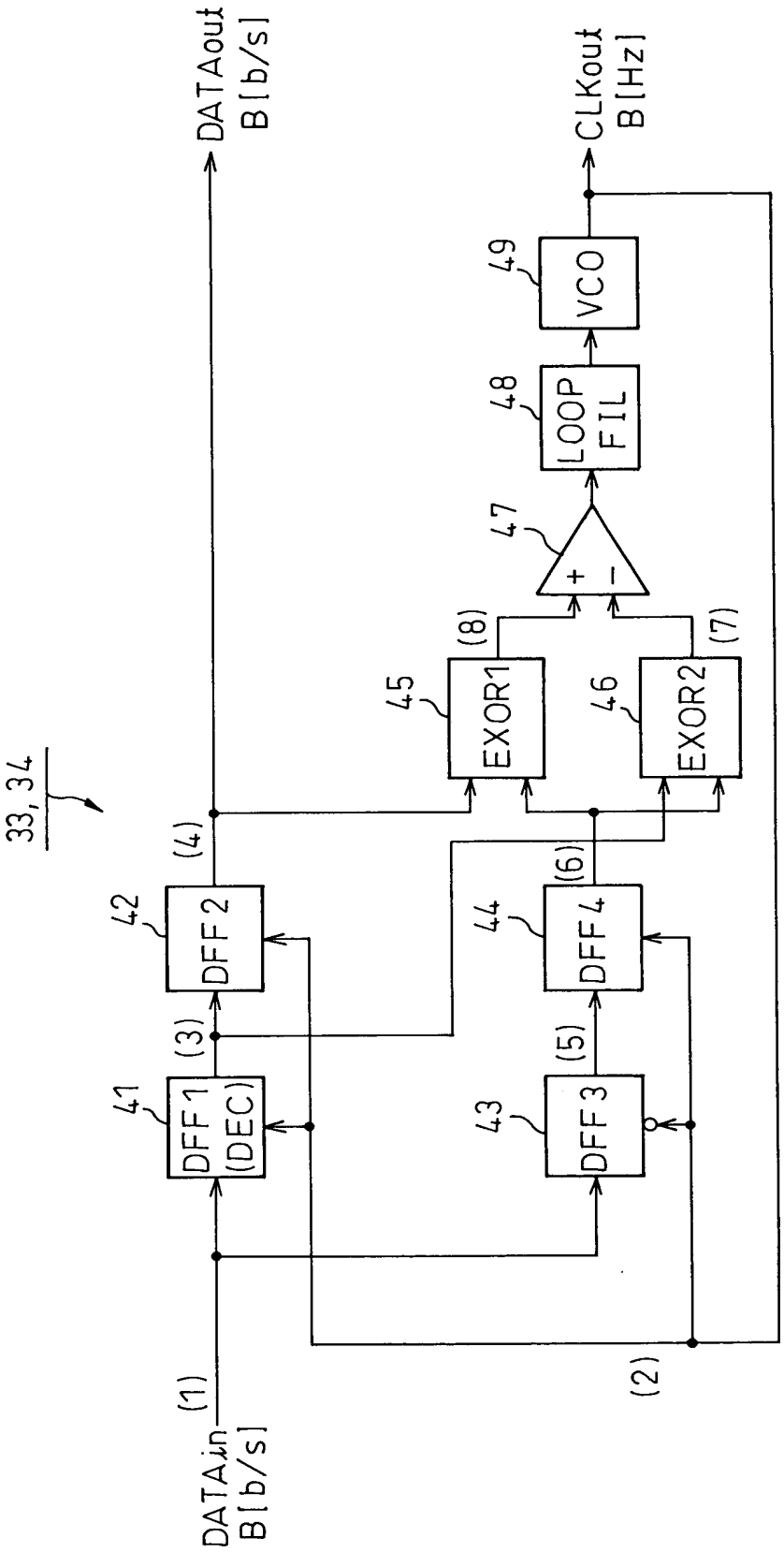

33, 34
DATAout
B [b/s]
CLKout
B [Hz]
DATAin
B [b/s]
(1)
(2)
(3)
(4)
(5)
(6)
(7)
(8)
41
DFF 1
(DEC)
42
DFF 2
43
DFF 3
44
DFF 4
45
EXOR1
46
EXOR2
47
+
−
48
LOOP
FIL
49
VCO

Fig.3

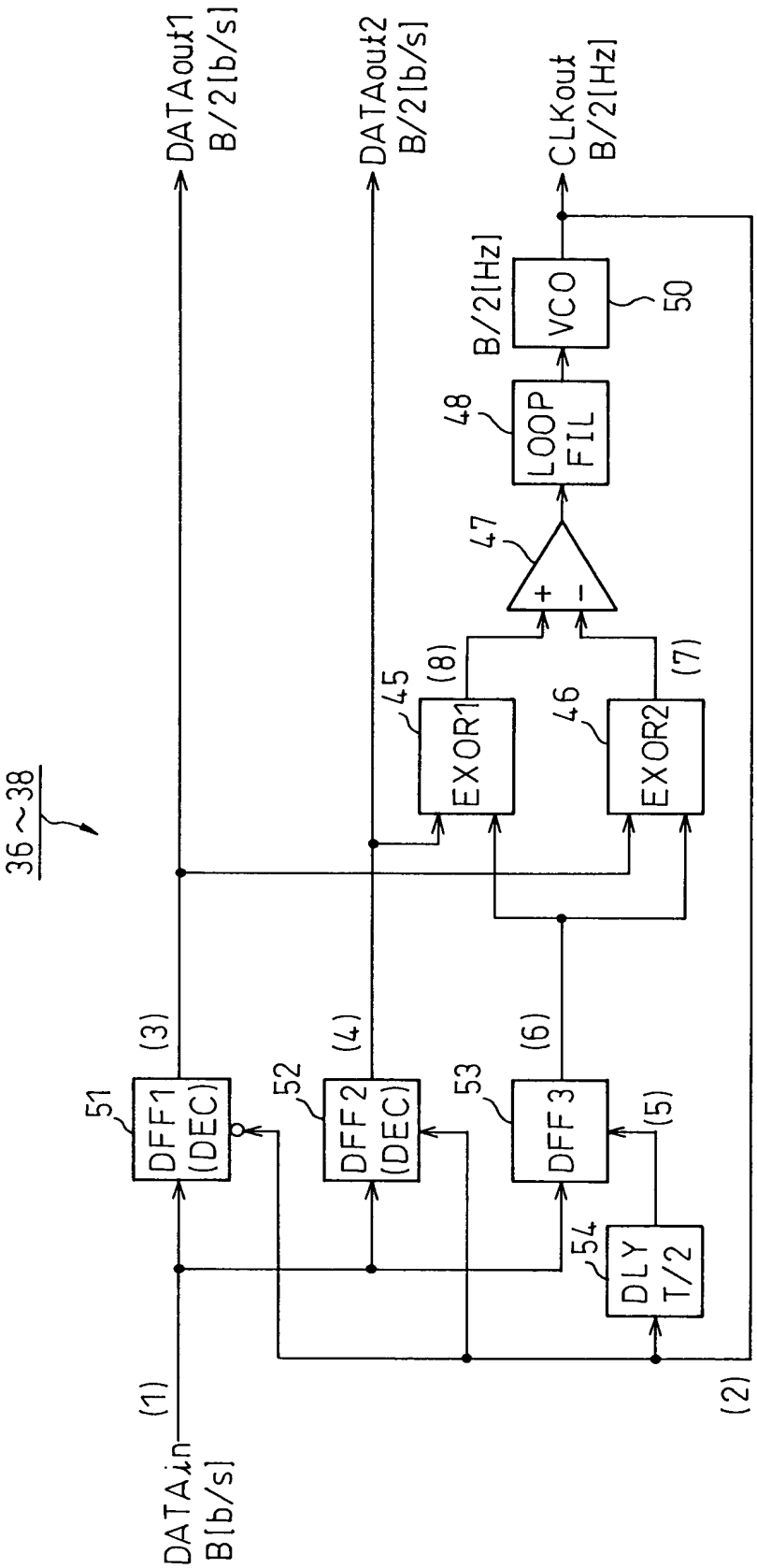

DATAout1
B/2[b/s]
DATAout2
B/2[b/s]
CLKout
B/2[Hz]
B/2[Hz]
VCO
50
48
LOOP
FIL
47
+
-
45
(8)
EXOR1
46
(7)
EXOR2
36~38
51
(3)
DFF1
(DEC)
52
(4)
DFF2
(DEC)
53
(6)
DFF3
(5)
54
DLY
T/2
(1)
DATAin
B[b/s]
(2)

Fig. 4

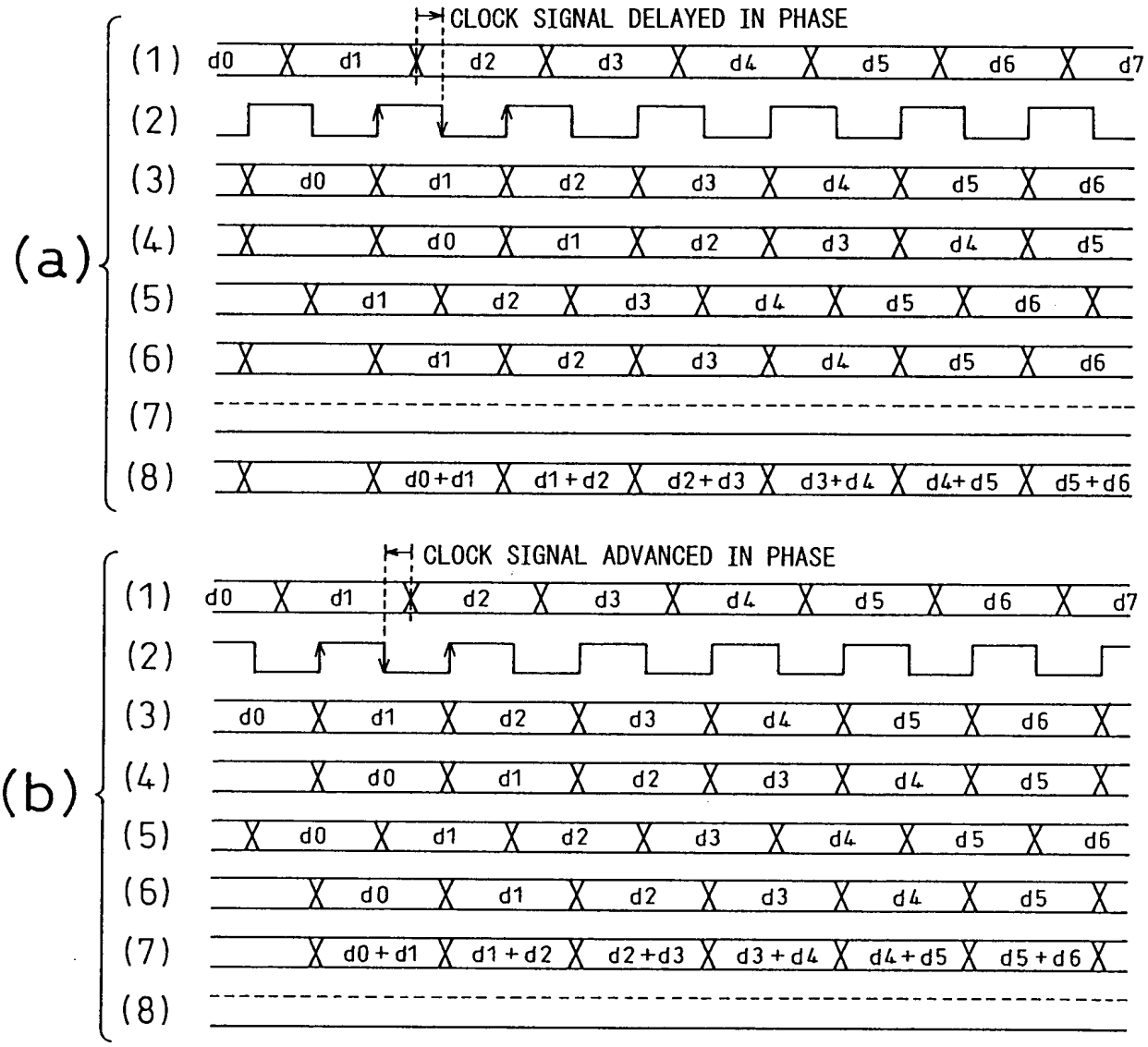

CLOCK SIGNAL DELAYED IN PHASE
(a)
(1) d0 d1 d2 d3 d4 d5 d6 d7
(2)
(3) d0 d1 d2 d3 d4 d5 d6
(4) d0 d1 d2 d3 d4 d5
(5) d1 d2 d3 d4 d5 d6
(6) d1 d2 d3 d4 d5 d6
(7)
(8) d0+d1 d1+d2 d2+d3 d3+d4 d4+d5 d5+d6
CLOCK SIGNAL ADVANCED IN PHASE
(b)
(1) d0 d1 d2 d3 d4 d5 d6 d7
(2)
(3) d0 d1 d2 d3 d4 d5 d6
(4) d0 d1 d2 d3 d4 d5
(5) d0 d1 d2 d3 d4 d5 d6
(6) d0 d1 d2 d3 d4 d5
(7) d0+d1 d1+d2 d2+d3 d3+d4 d4+d5 d5+d6
(8)

Fig.5

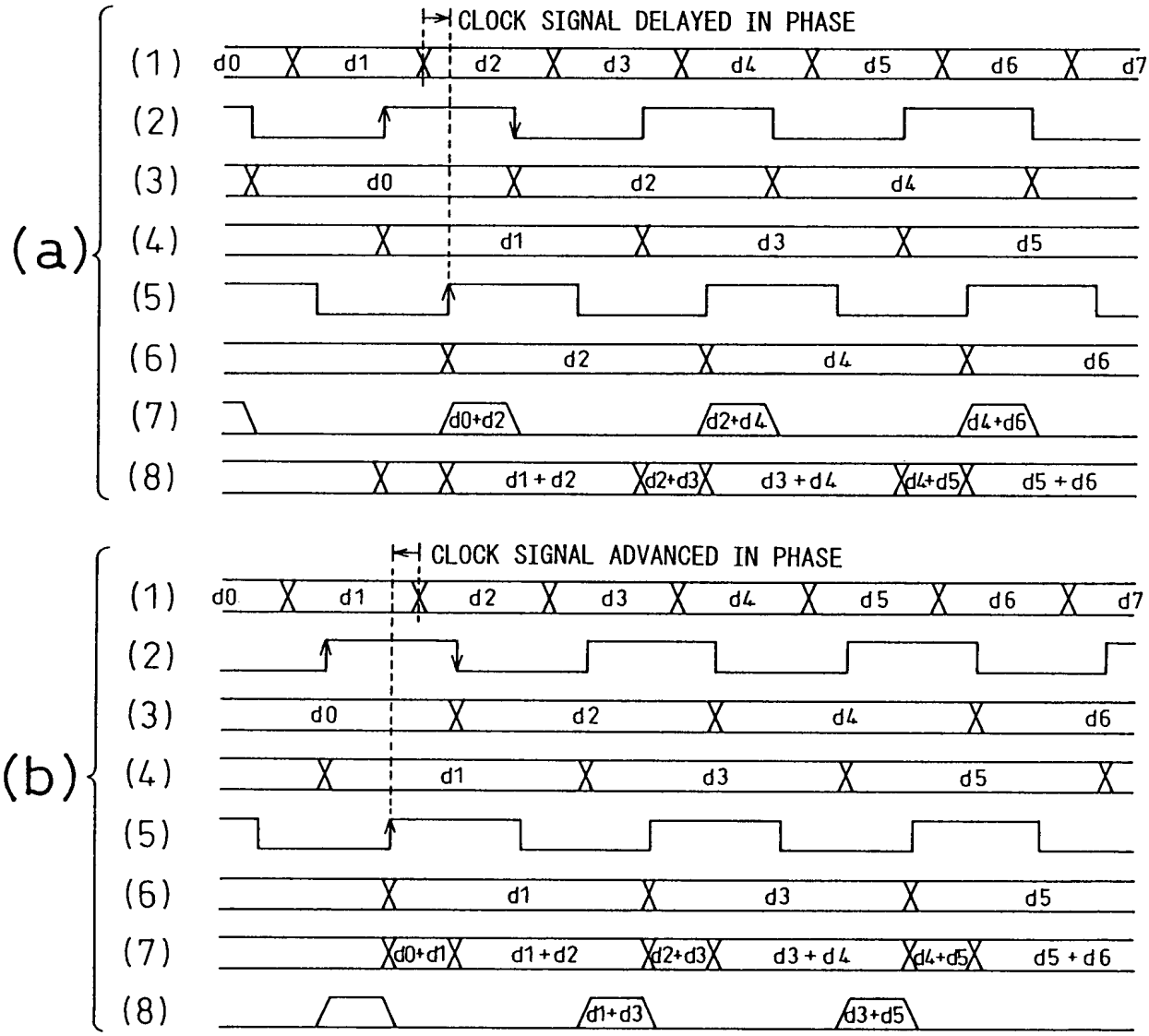

(a)
CLOCK SIGNAL DELAYED IN PHASE
(1)
d0
d1
d2
d3
d4
d5
d6
d7
(2)
(3)
d0
d2
d4
(4)
d1
d3
d5
(5)
(6)
d2
d4
d6
(7)
d0+d2
d2+d4
d4+d6
(8)
d1+d2
d2+d3
d3+d4
d4+d5
d5+d6
(b)
CLOCK SIGNAL ADVANCED IN PHASE
(1)
d0
d1
d2
d3
d4
d5
d6
d7
(2)
(3)
d0
d2
d4
d6
(4)
d1
d3
d5
(5)
(6)
d1
d3
d5
(7)
d0+d1
d1+d2
d2+d3
d3+d4
d4+d5
d5+d6
(8)
d1+d3
d3+d5

Fig.6

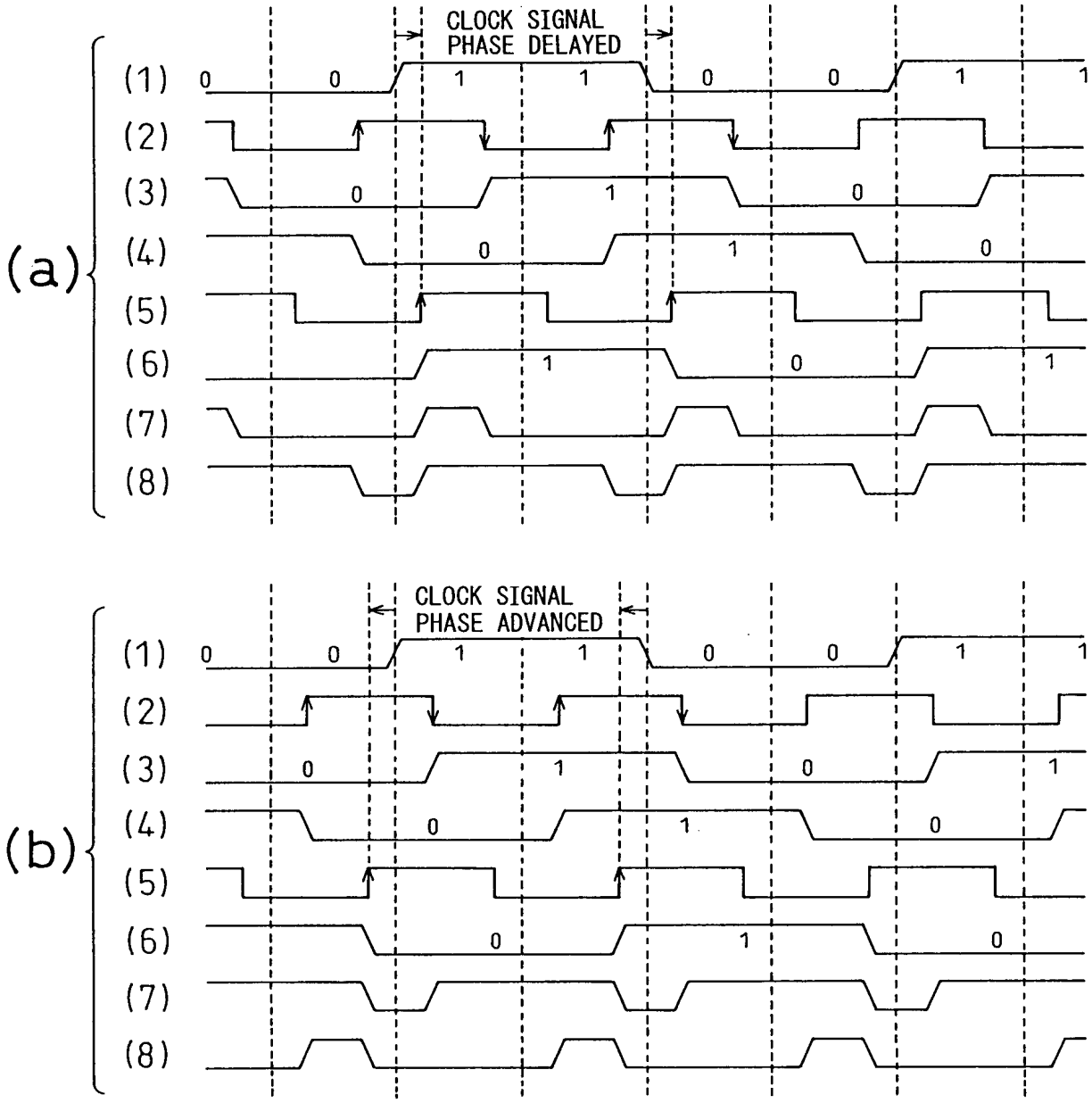

(a)
(1)
(2)
(3)
(4)
(5)
(6)
(7)
(8)
CLOCK SIGNAL
PHASE DELAYED
(b)
(1)
(2)
(3)
(4)
(5)
(6)
(7)
(8)
CLOCK SIGNAL
PHASE ADVANCED

Fig.7

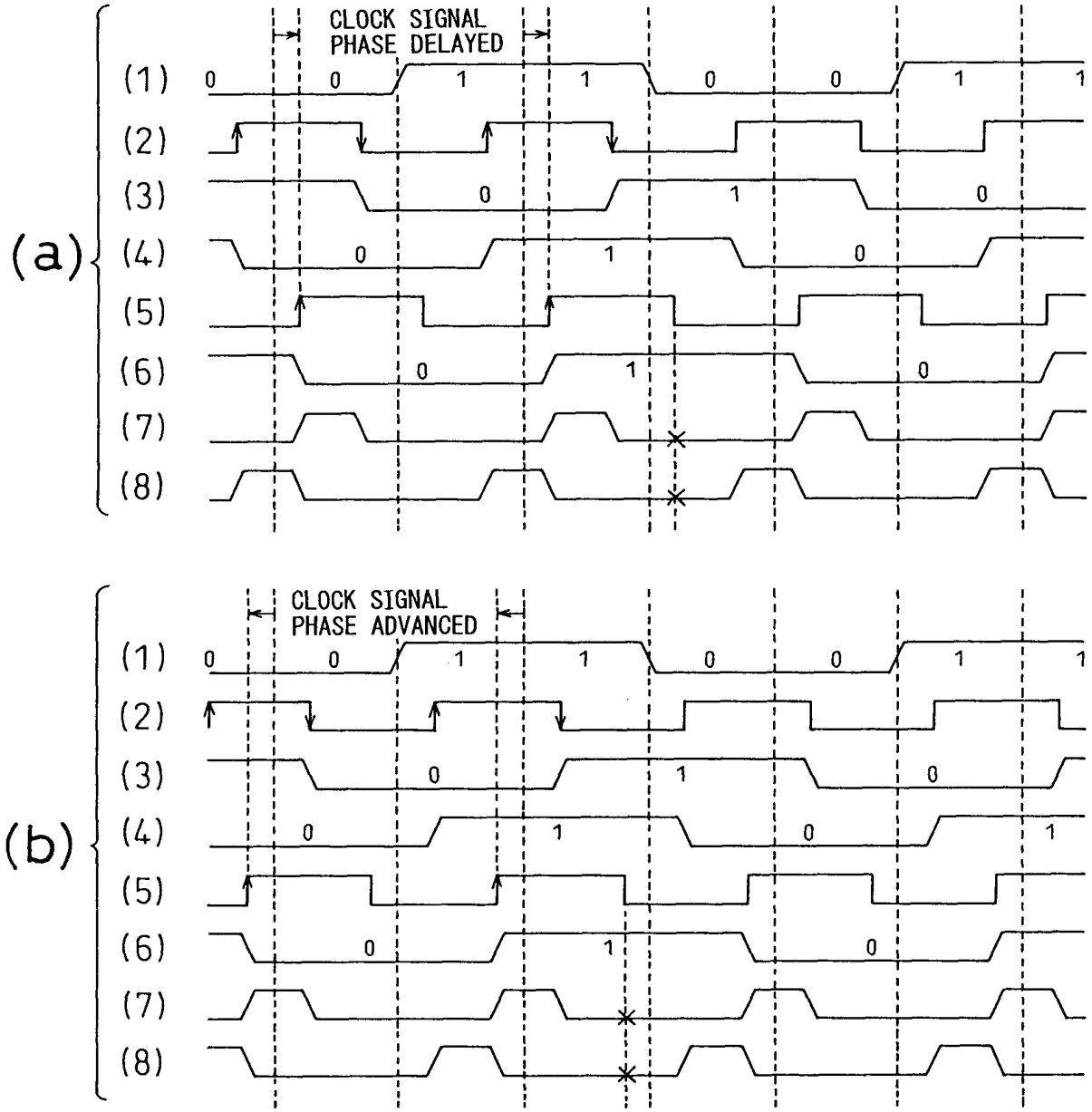

(a)
CLOCK SIGNAL
PHASE DELAYED
(1)
(2)
(3)
(4)
(5)
(6)
(7)
(8)
(b)
CLOCK SIGNAL
PHASE ADVANCED
(1)
(2)
(3)
(4)
(5)
(6)
(7)
(8)

Fig.8

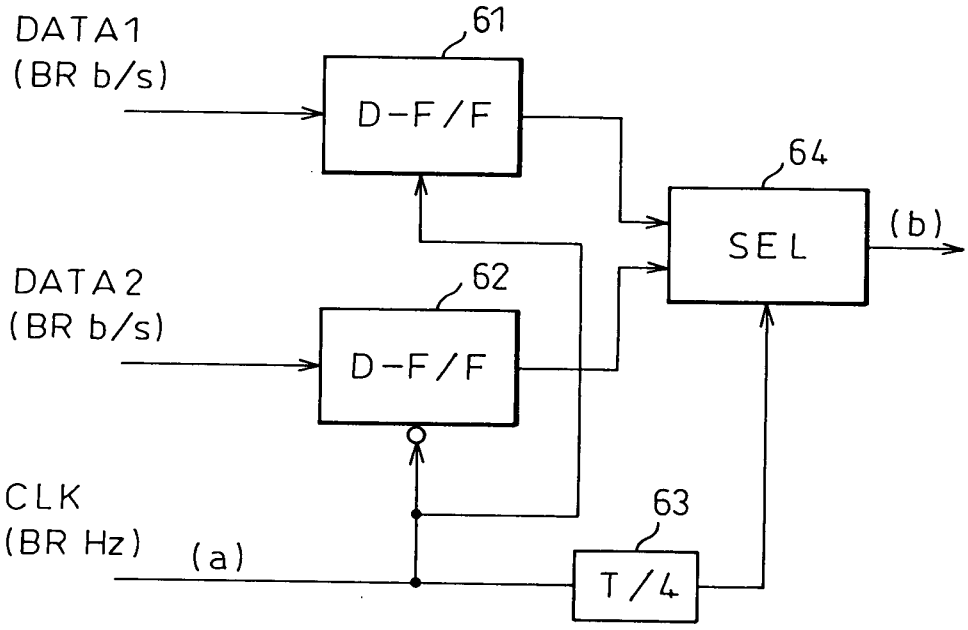


Fig.9

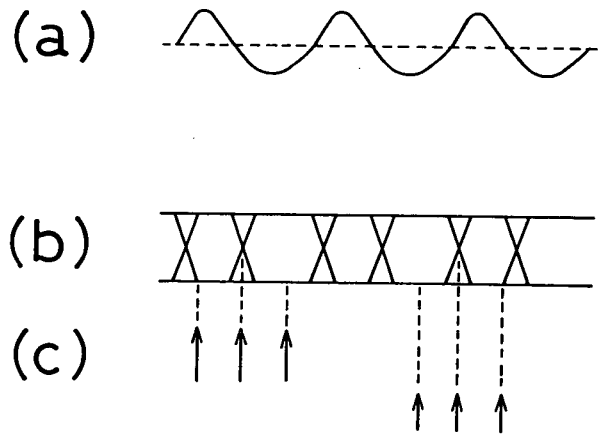


Fig. 10

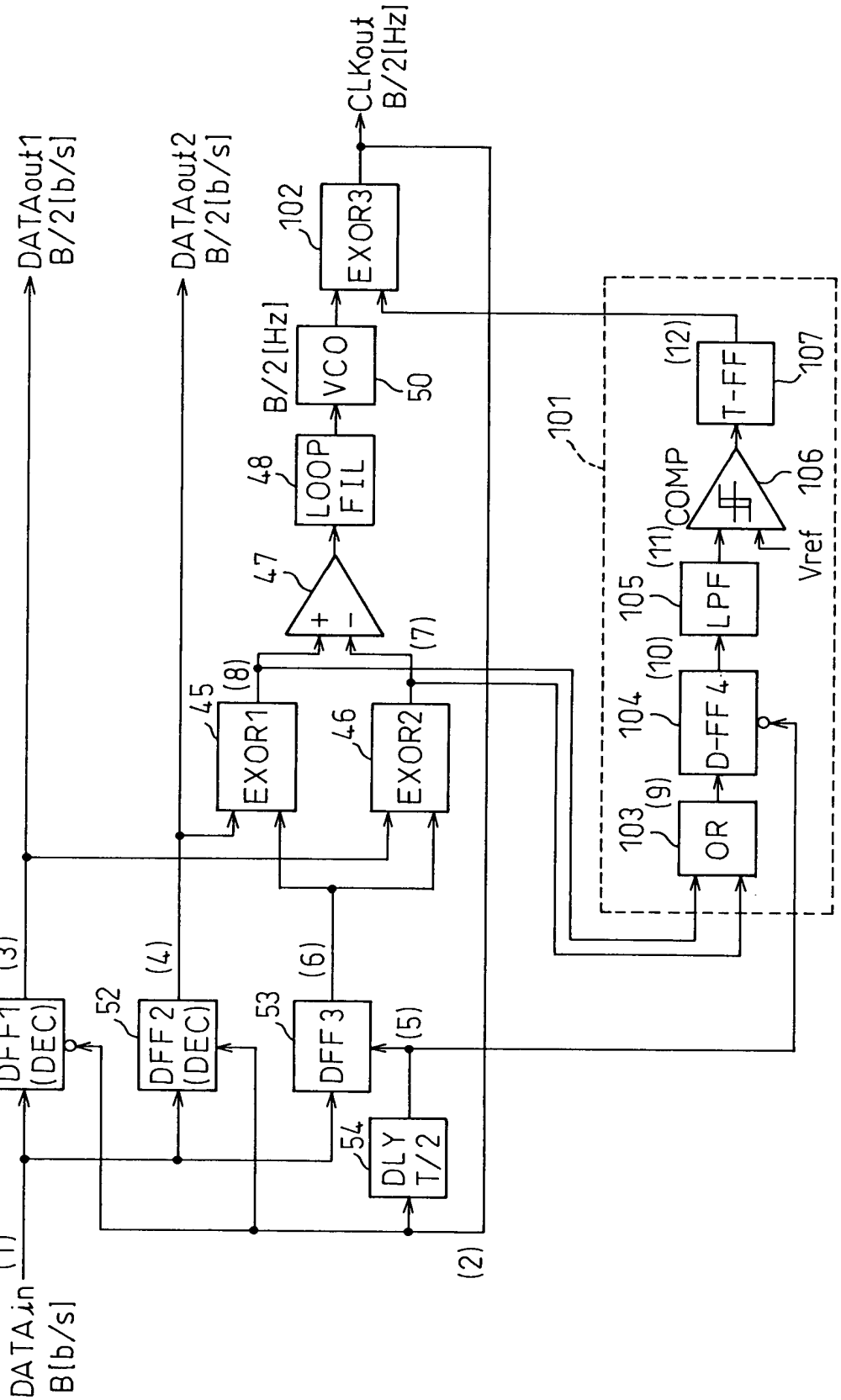

DATAin
B[b/s]
(1)
DFF1
(DEC)
51
(3)
DFF2
(DEC)
52
(4)
DFF3
53
(6)
DLY
T/2
54
(5)
(2)
DATAout1
B/2[b/s]
DATAout2
B/2[b/s]
EXOR1
45
(8)
EXOR2
46
(7)
47
+
−
LOOP
FIL
48
B/2[Hz]
VCO
50
EXOR3
102
CLKout
B/2[Hz]
101
OR
103
(9)
D-FF 4
104
(10)
LPF
105
(11)
COMP
106
Vref
T-FF
107
(12)

Fig.11

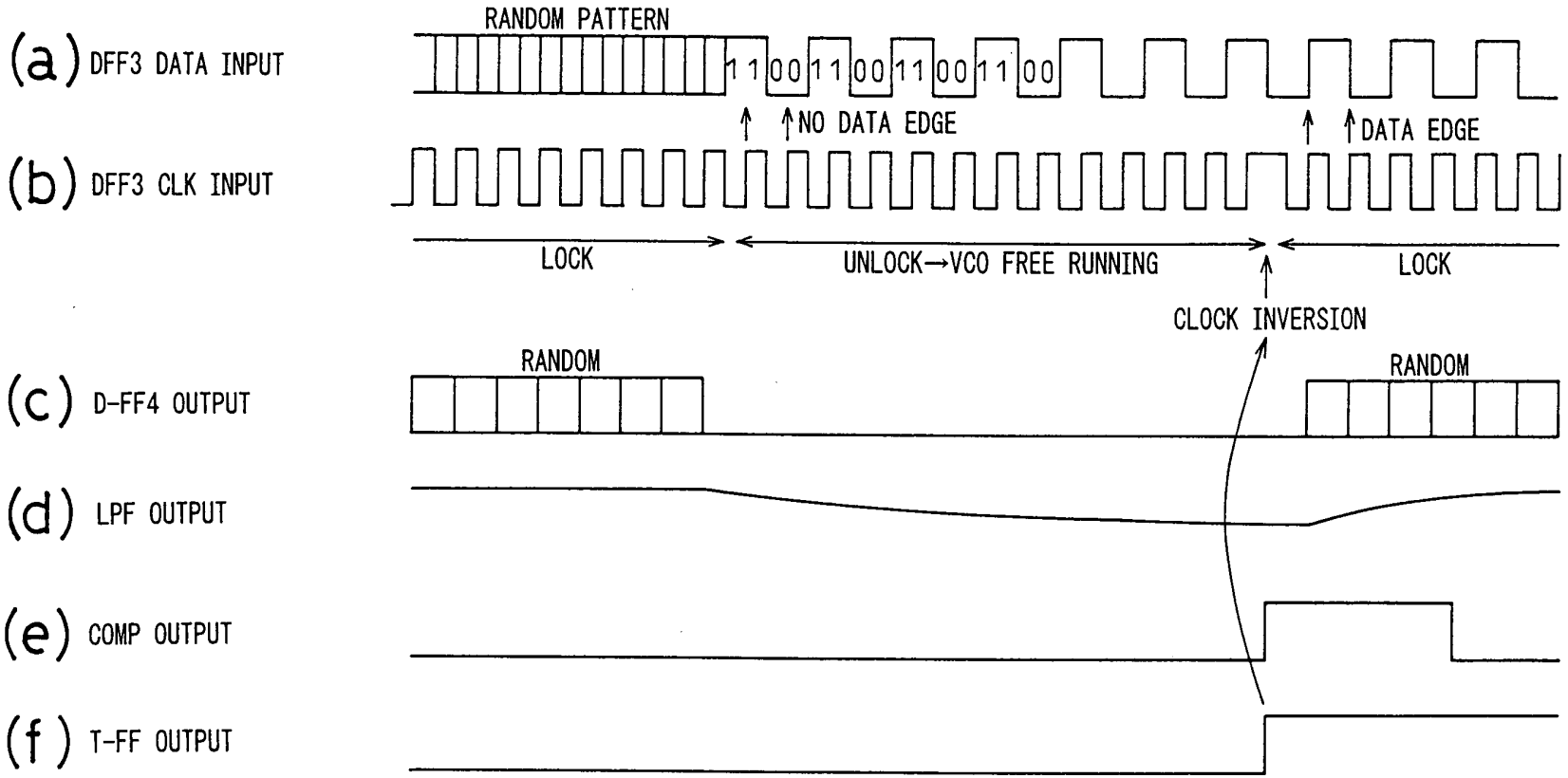

(a) DFF3 DATA INPUT
RANDOM PATTERN
1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0
NO DATA EDGE
DATA EDGE
(b) DFF3 CLK INPUT
LOCK
UNLOCK→VCO FREE RUNNING
LOCK
CLOCK INVERSION
RANDOM
RANDOM
(c) D-FF4 OUTPUT
(d) LPF OUTPUT
(e) COMP OUTPUT
(f) T-FF OUTPUT

Fig.12

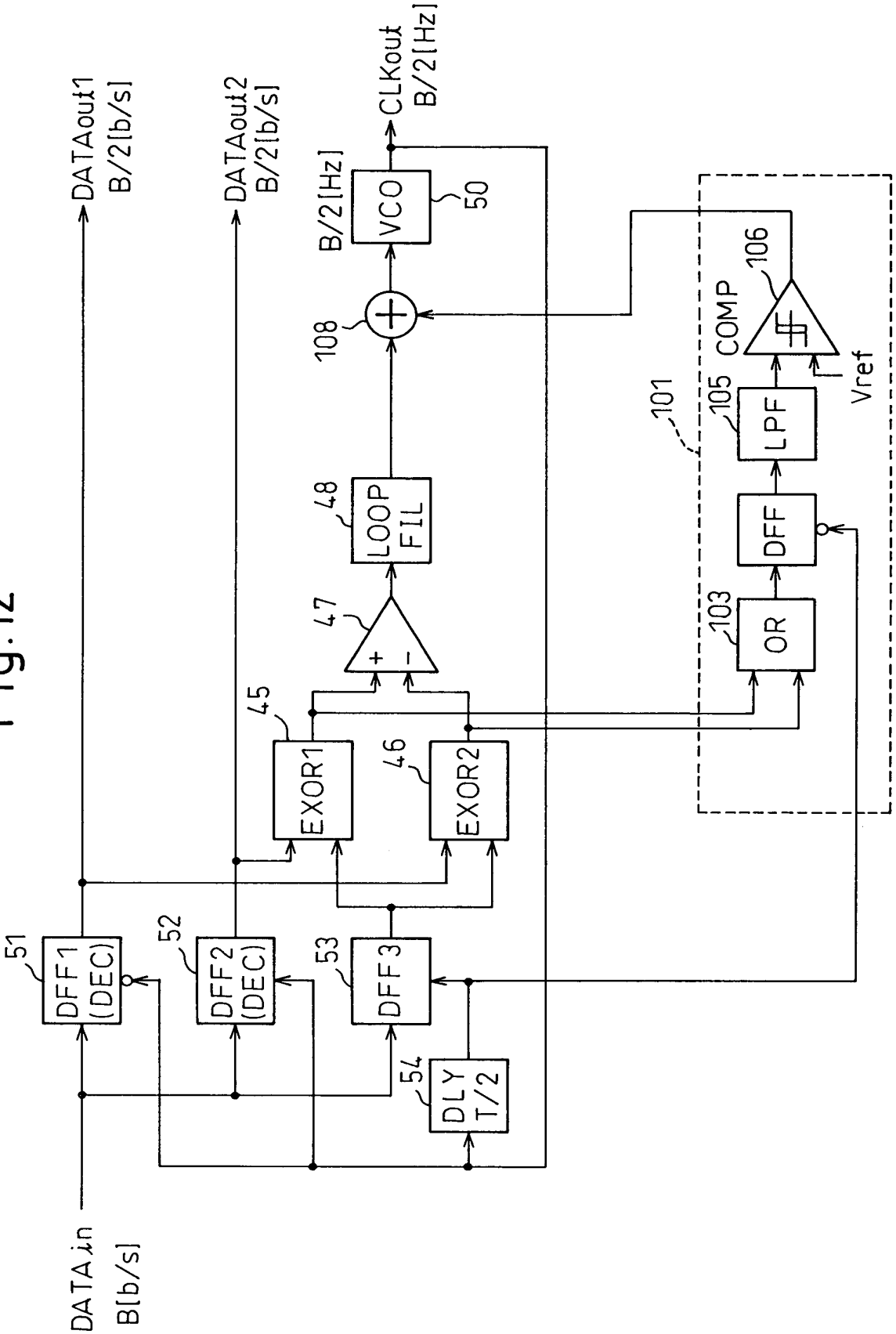

DATAout1
B/2[b/s]
DATAout2
B/2[b/s]
CLKout
B/2[Hz]
B/2[Hz]
VCO
50
108
48
LOOP
FIL
47
+
-
45
EXOR1
46
EXOR2
51
DFF1
(DEC)
52
DFF2
(DEC)
53
DFF3
54
DLY
T/2
DATAin
B[b/s]
101
105
LPF
106
COMP
Vref
103
OR
DFF

Fig.13

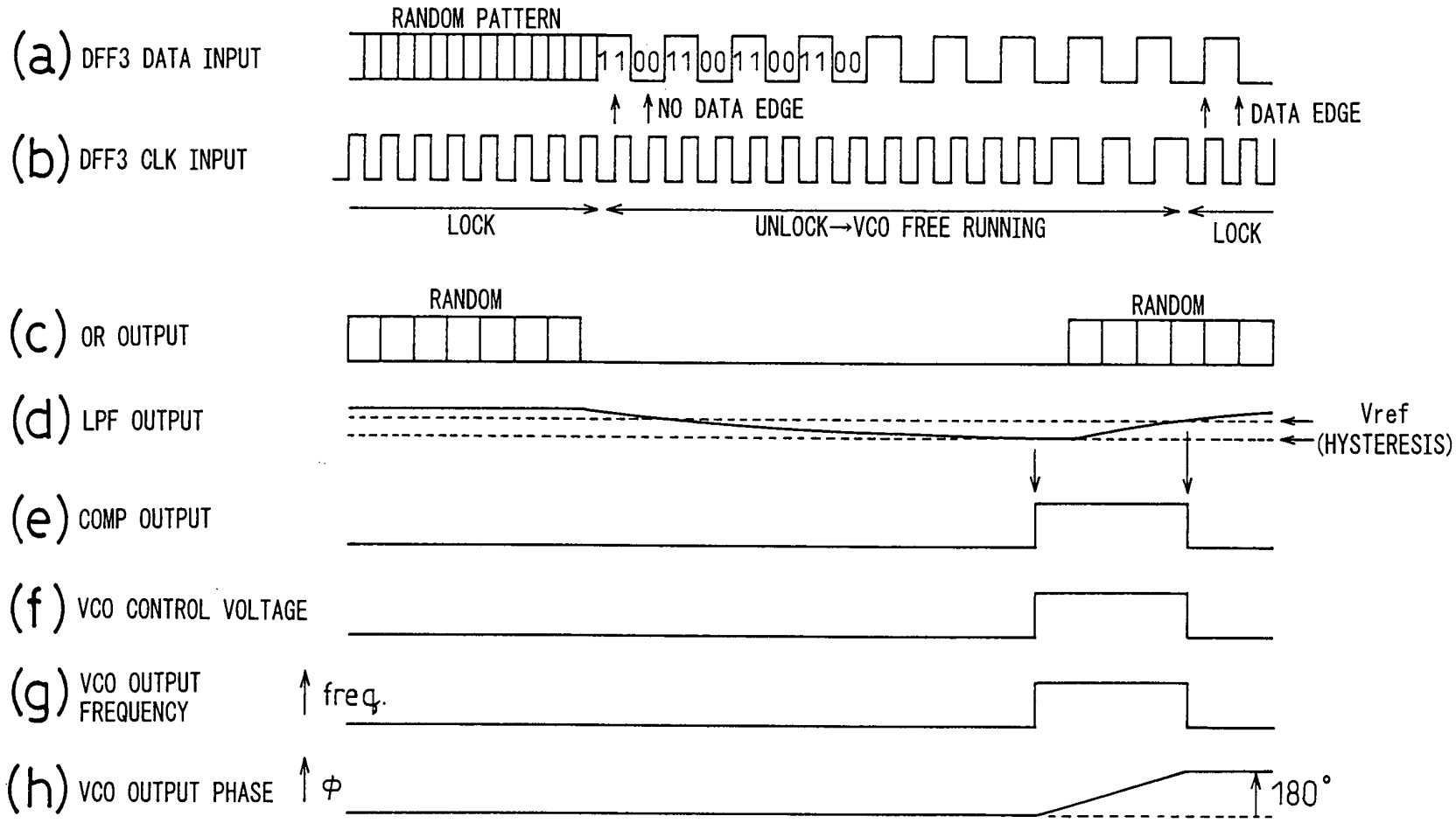

(a) DFF3 DATA INPUT
RANDOM PATTERN
1100110011001100
NO DATA EDGE
DATA EDGE
(b) DFF3 CLK INPUT
LOCK
UNLOCK→VCO FREE RUNNING
LOCK
(c) OR OUTPUT
RANDOM
RANDOM
(d) LPF OUTPUT
Vref
(HYSTERESIS)
(e) COMP OUTPUT
(f) VCO CONTROL VOLTAGE
(g) VCO OUTPUT FREQUENCY
freq.
(h) VCO OUTPUT PHASE
Φ
180°

Fig.14

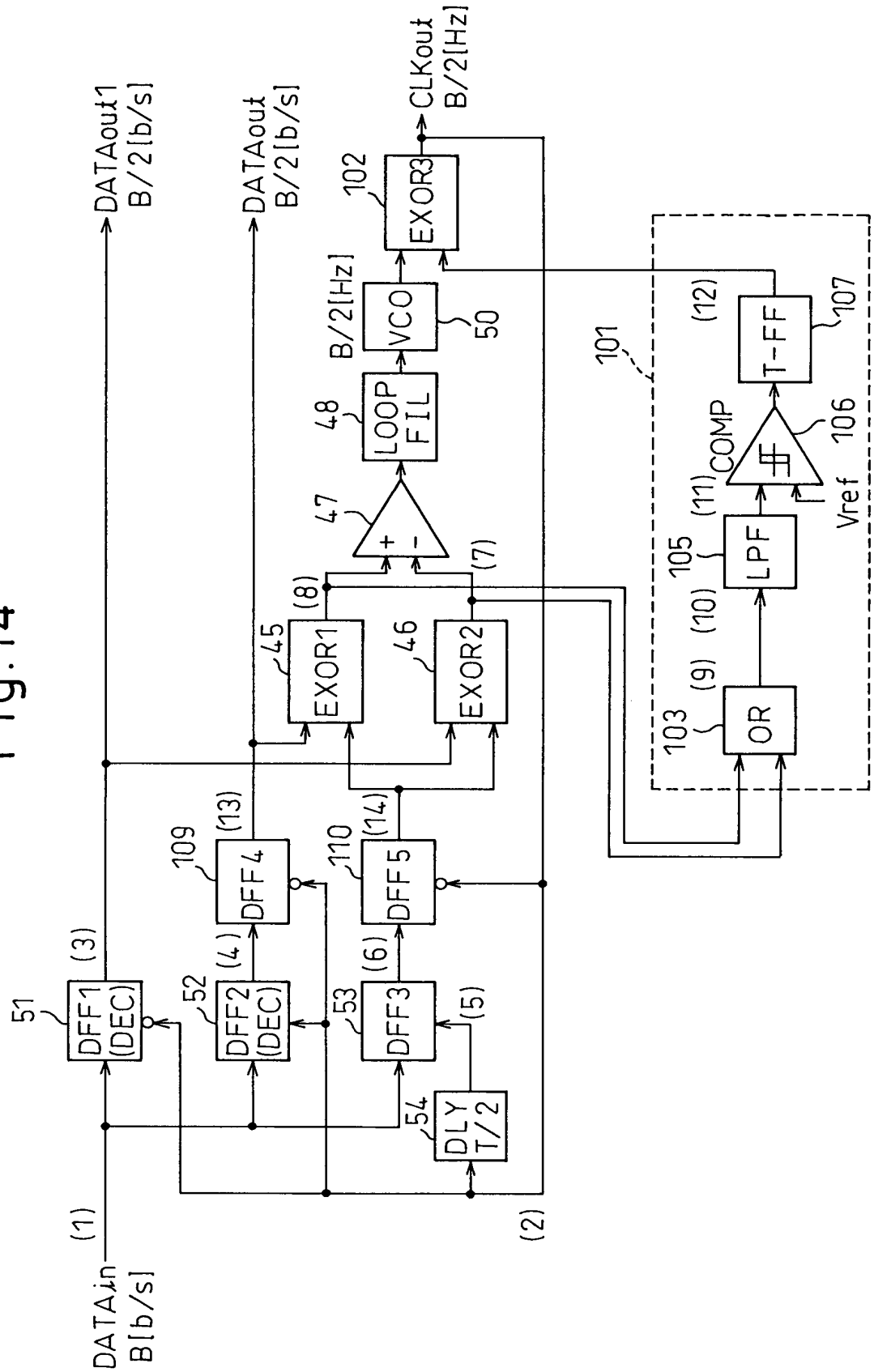

DATAin
B[b/s]
(1)
DATAout1
B/2[b/s]
DATAout
B/2[b/s]
CLKout
B/2[Hz]
B/2[Hz]
(2)
51
DFF1
(DEC)
(3)
52
DFF2
(DEC)
(4)
53
DFF3
(6)
(5)
54
DLY
T/2
109
DFF4
(13)
110
DFF5
(14)
45
EXOR1
(8)
46
EXOR2
(7)
47
+
-
48
LOOP
FIL
VCO
50
102
EXOR3
101
103
OR
(9)
(10)
105
LPF
(11)
COMP
106
Vref
(12)
T-FF
107

Fig.15

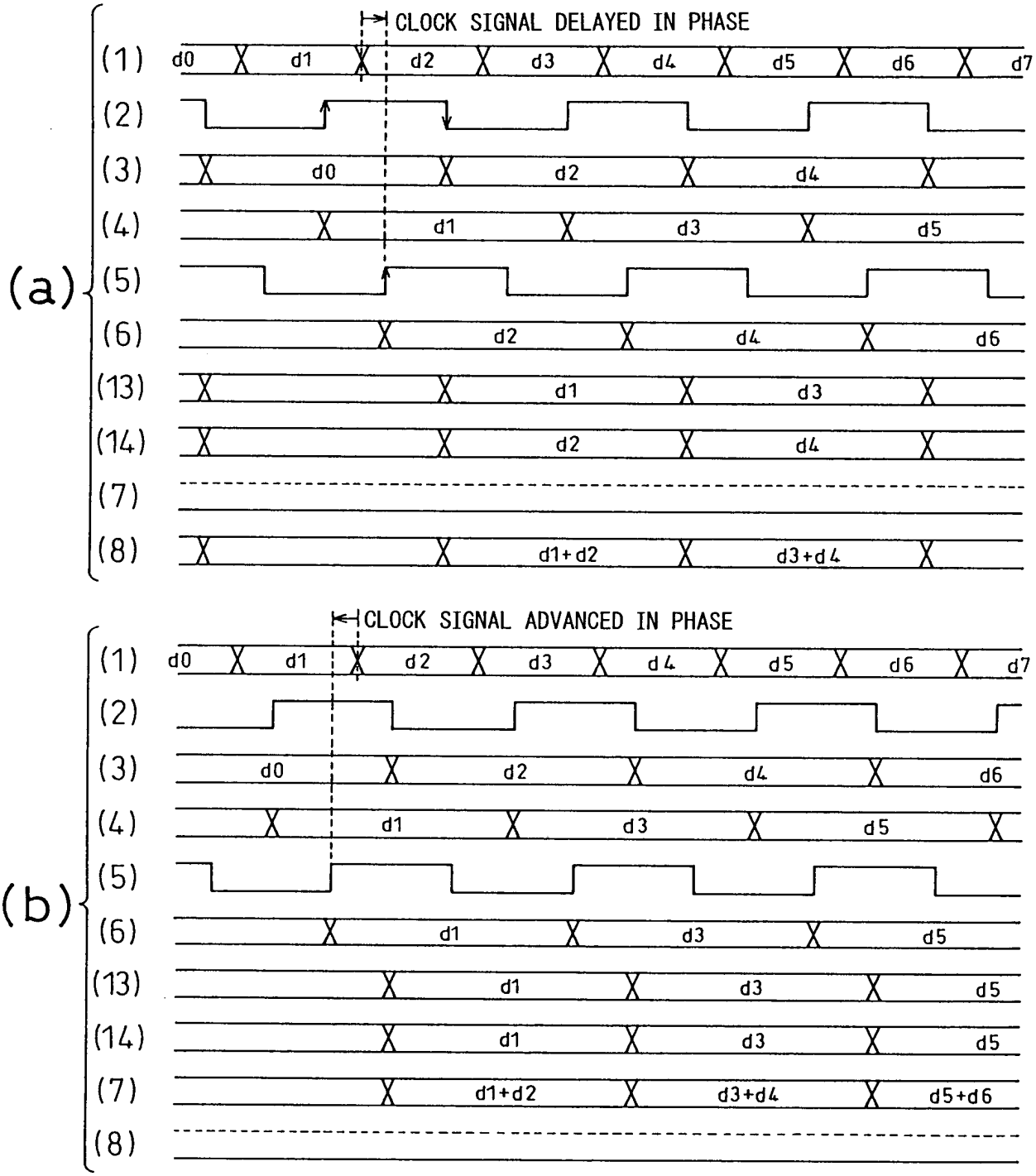

CLOCK SIGNAL DELAYED IN PHASE
(1)
(2)
(3)
(4)
(5)
(6)
(13)
(14)
(7)
(8)
(a)
d0
d1
d2
d3
d4
d5
d6
d7
d1+d2
d3+d4
CLOCK SIGNAL ADVANCED IN PHASE
(b)
d5+d6

Fig.16

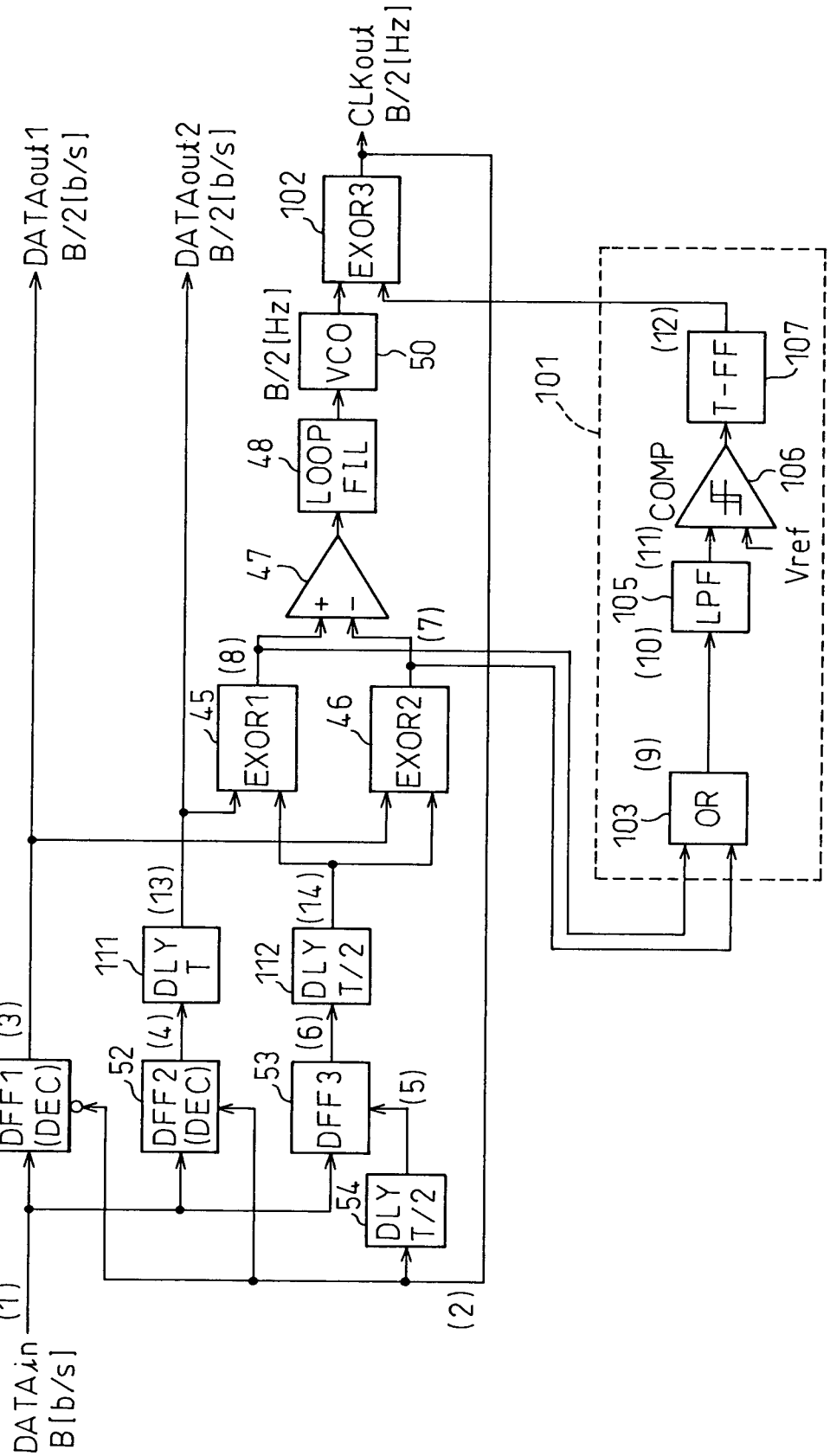

DATAin
B[b/s]
(1)
DFF1
(DEC)
51
(3)
DFF2
(DEC)
52
(4)
DFF3
53
(6)
(5)
DLY
T/2
54
DLY
T
111
(13)
DLY
T/2
112
(14)
(2)
EXOR1
45
(8)
EXOR2
46
(7)
47
+
-
LOOP
FIL
48
B/2[Hz]
VCO
50
EXOR3
102
CLKout
B/2[Hz]
DATAout1
B/2[b/s]
DATAout2
B/2[b/s]
101
OR
103
(9)
LPF
105
(10)
(11)
COMP
106
Vref
T-FF
107
(12)

Fig.17

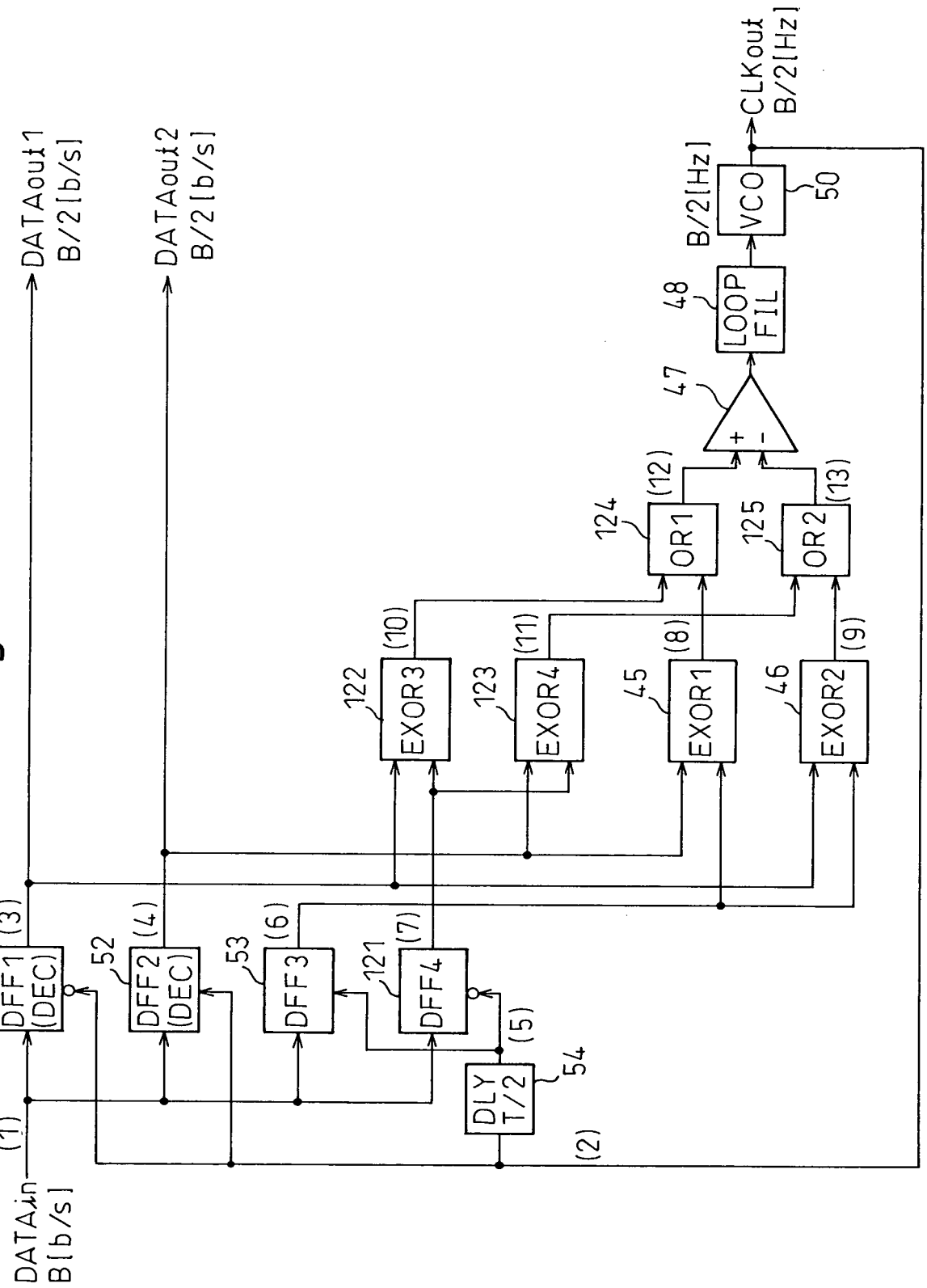

DATAin
B[b/s]
(1)
DFF1
(DEC)
51
(3)
DFF2
(DEC)
52
(4)
DFF3
53
(6)
DFF4
121
(7)
DLY
T/2
54
(5)
(2)
DATAout1
B/2[b/s]
DATAout2
B/2[b/s]
EXOR3
122
(10)
EXOR4
123
(11)
EXOR1
45
(8)
EXOR2
46
(9)
OR1
124
(12)
OR2
125
(13)
47
+
-
LOOP
FIL
48
B/2[Hz]
VCO
50
CLKout
B/2[Hz]

Fig.18

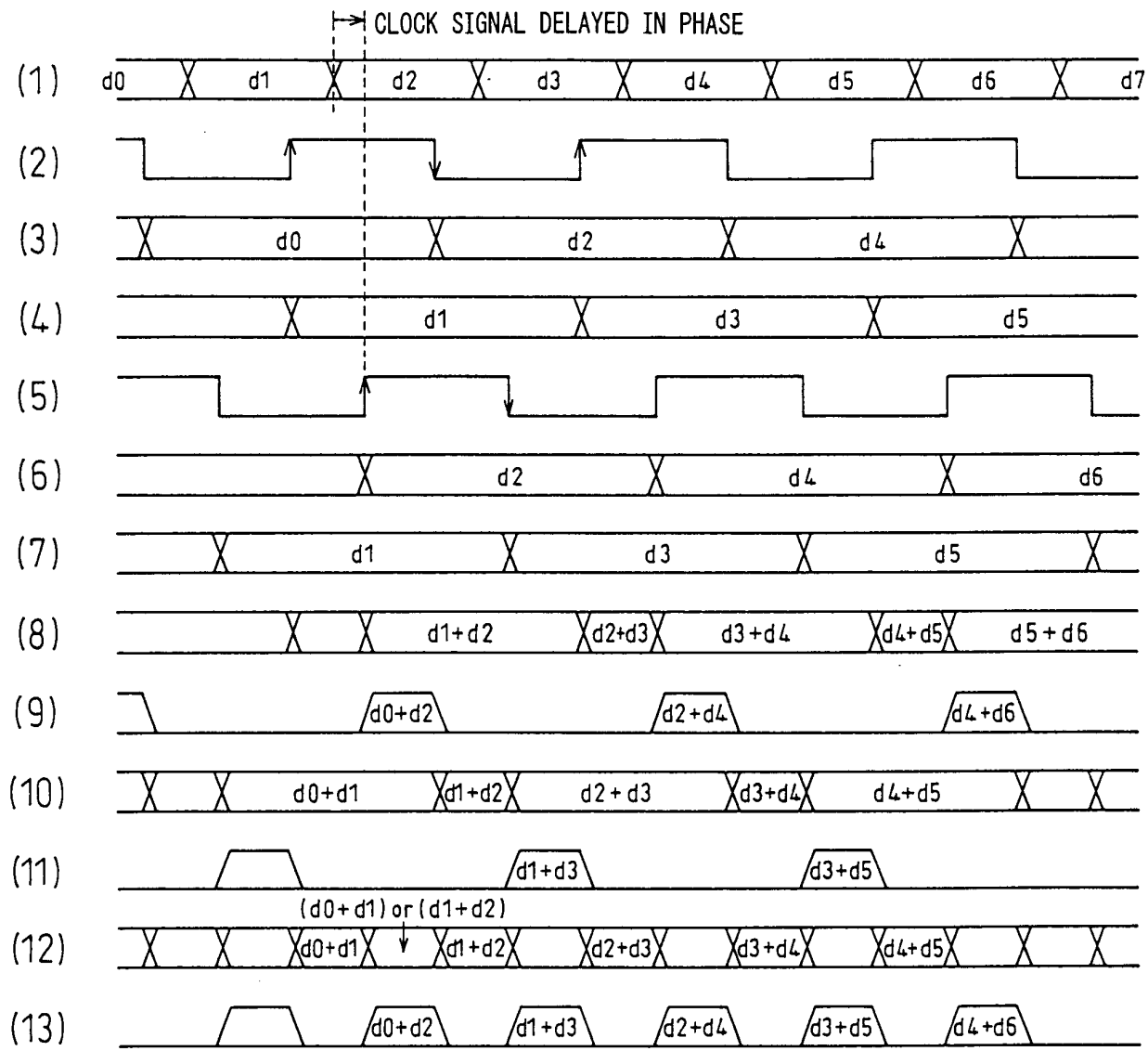

CLOCK SIGNAL DELAYED IN PHASE
(1)
d0
d1
d2
d3
d4
d5
d6
d7
(2)
(3)
d0
d2
d4
(4)
d1
d3
d5
(5)
(6)
d2
d4
d6
(7)
d1
d3
d5
(8)
d1+d2
d2+d3
d3+d4
d4+d5
d5+d6
(9)
d0+d2
d2+d4
d4+d6
(10)
d0+d1
d1+d2
d2+d3
d3+d4
d4+d5
(11)
d1+d3
d3+d5
(d0+d1) or (d1+d2)
(12)
d0+d1
d1+d2
d2+d3
d3+d4
d4+d5
(13)
d0+d2
d1+d3
d2+d4
d3+d5
d4+d6

Fig.19

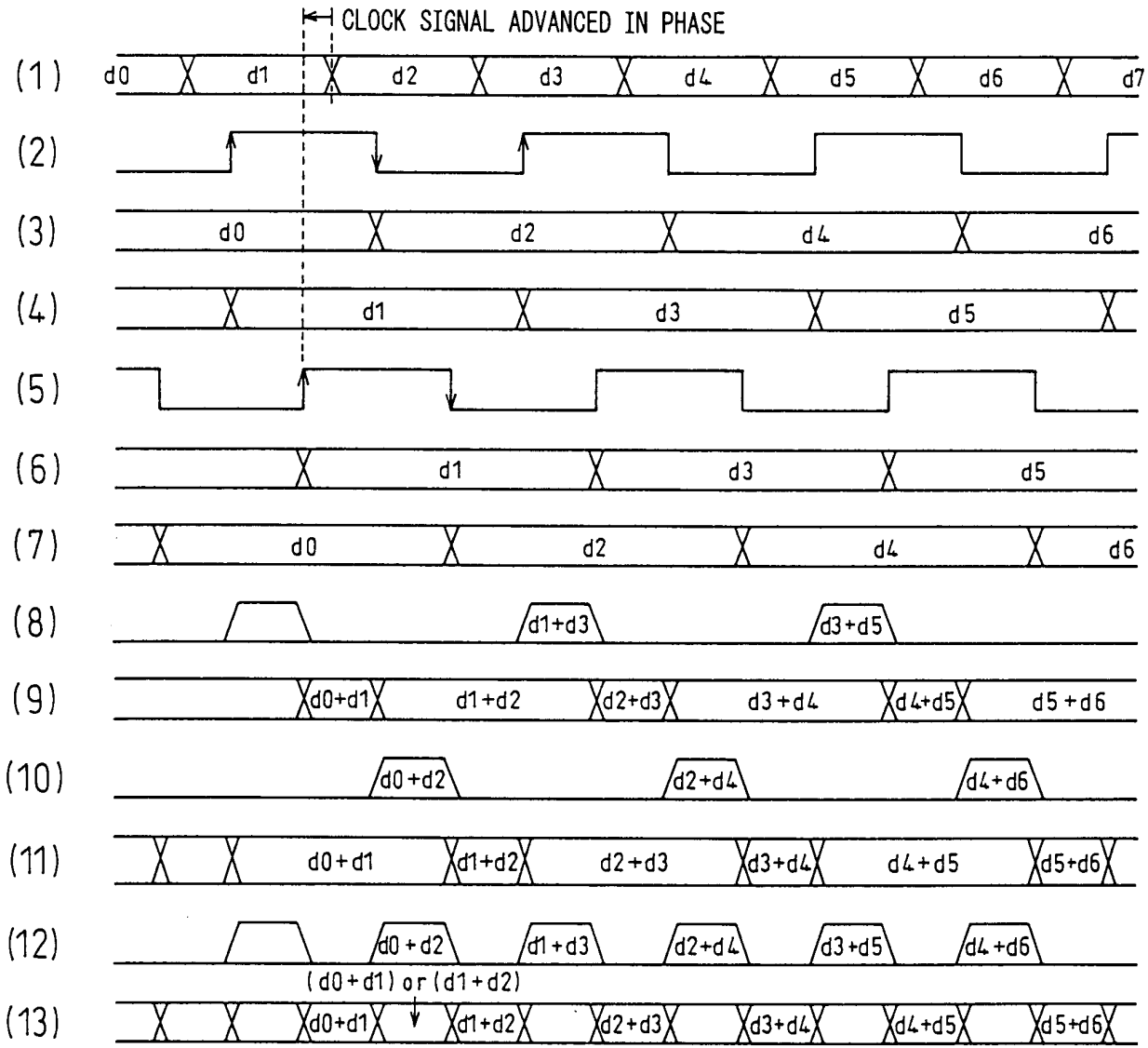

CLOCK SIGNAL ADVANCED IN PHASE
(1)
d0
d1
d2
d3
d4
d5
d6
d7
(2)
(3)
d0
d2
d4
d6
(4)
d1
d3
d5
(5)
(6)
d1
d3
d5
(7)
d0
d2
d4
d6
(8)
d1+d3
d3+d5
(9)
d0+d1
d1+d2
d2+d3
d3+d4
d4+d5
d5+d6
(10)
d0+d2
d2+d4
d4+d6
(11)
d0+d1
d1+d2
d2+d3
d3+d4
d4+d5
d5+d6
(12)
d0+d2
d1+d3
d2+d4
d3+d5
d4+d6
(d0+d1) or (d1+d2)
(13)
d0+d1
d1+d2
d2+d3
d3+d4
d4+d5
d5+d6

Fig.20

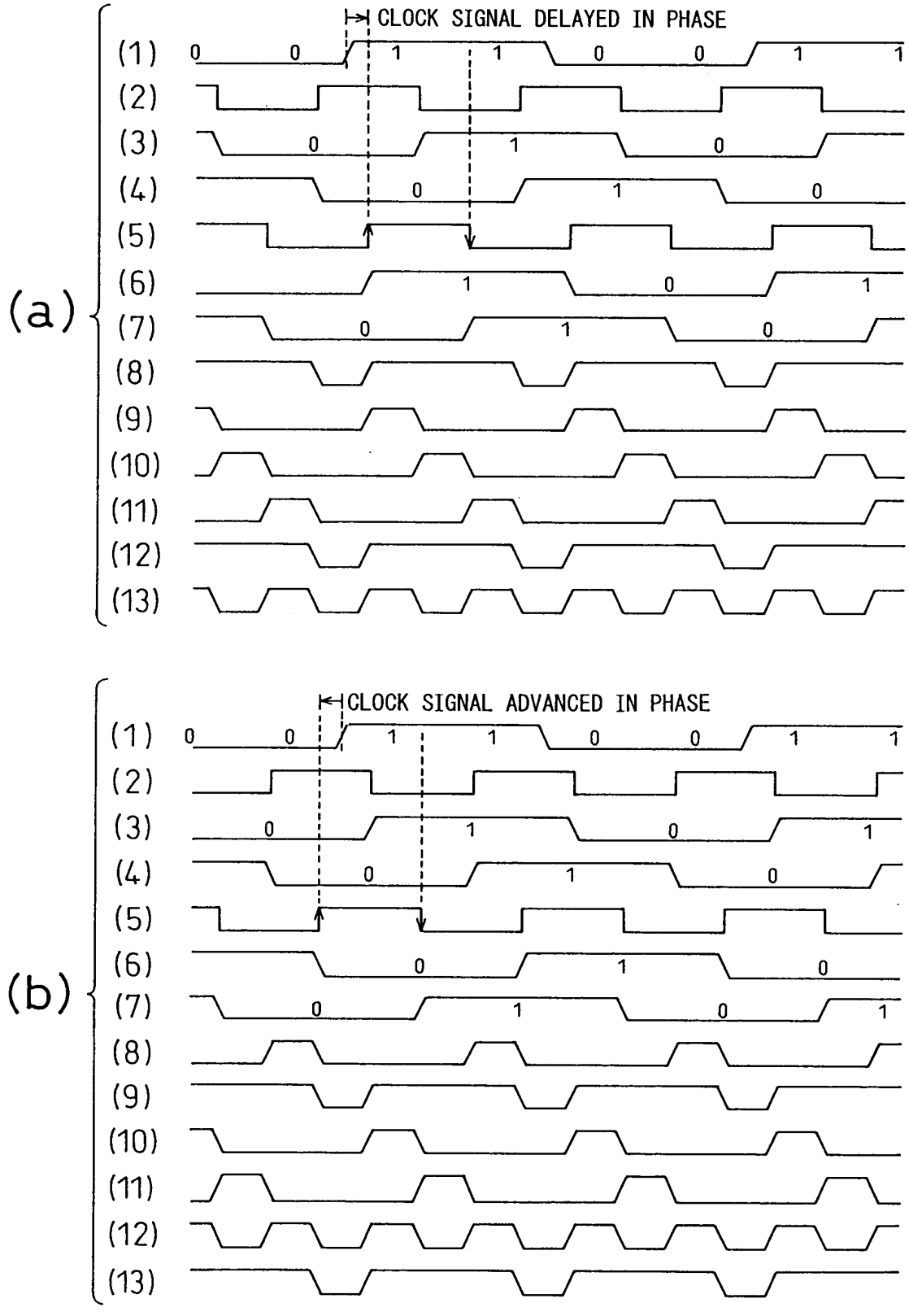

CLOCK SIGNAL DELAYED IN PHASE
(a)
(1)
(2)
(3)
(4)
(5)
(6)
(7)
(8)
(9)
(10)
(11)
(12)
(13)
CLOCK SIGNAL ADVANCED IN PHASE
(b)
(1)
(2)
(3)
(4)
(5)
(6)
(7)
(8)
(9)
(10)
(11)
(12)
(13)

Fig. 21

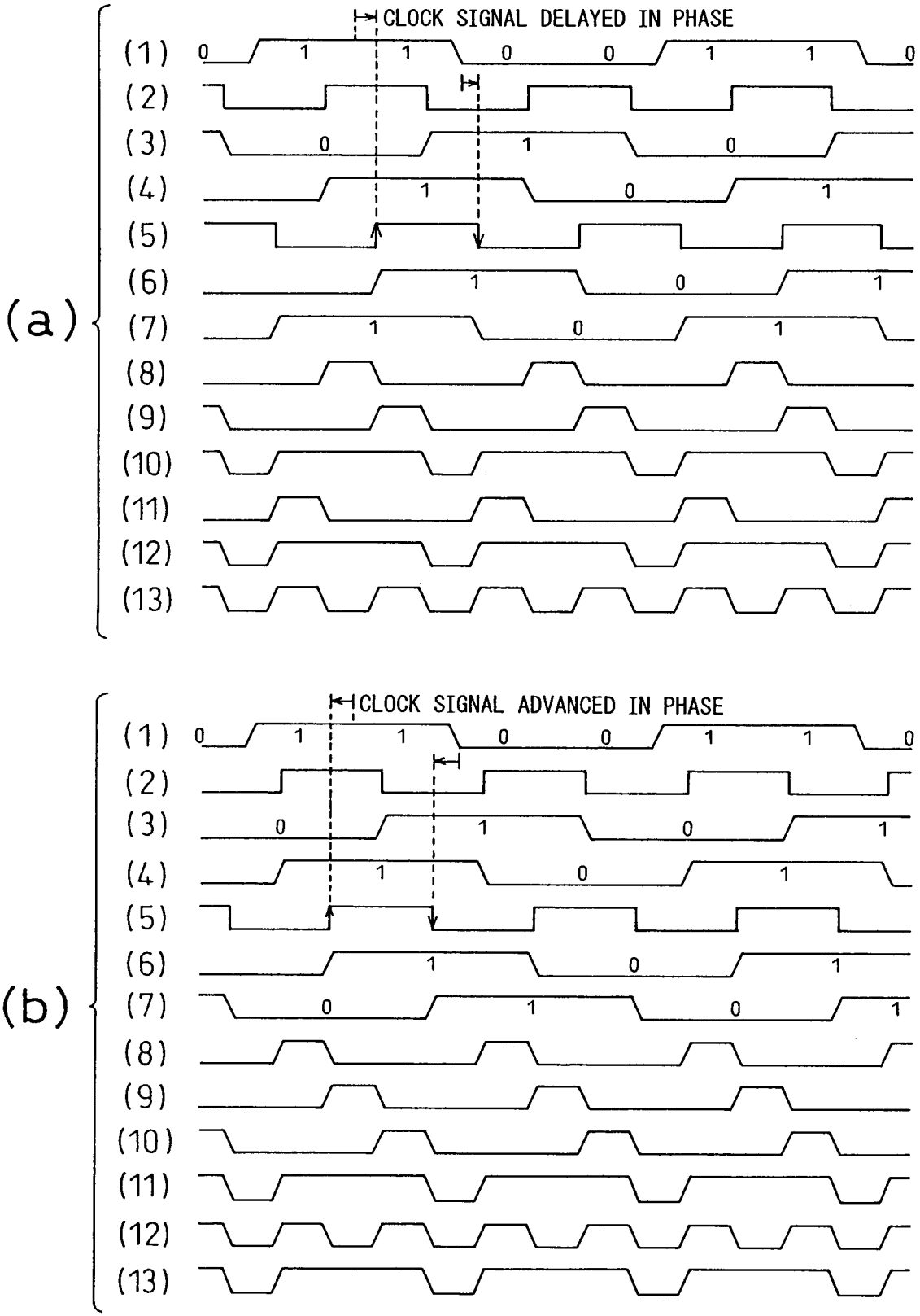

(a)
CLOCK SIGNAL DELAYED IN PHASE
(1)
(2)
(3)
(4)
(5)
(6)
(7)
(8)
(9)
(10)
(11)
(12)
(13)
(b)
CLOCK SIGNAL ADVANCED IN PHASE
(1)
(2)
(3)
(4)
(5)
(6)
(7)
(8)
(9)
(10)
(11)
(12)
(13)

Fig. 22

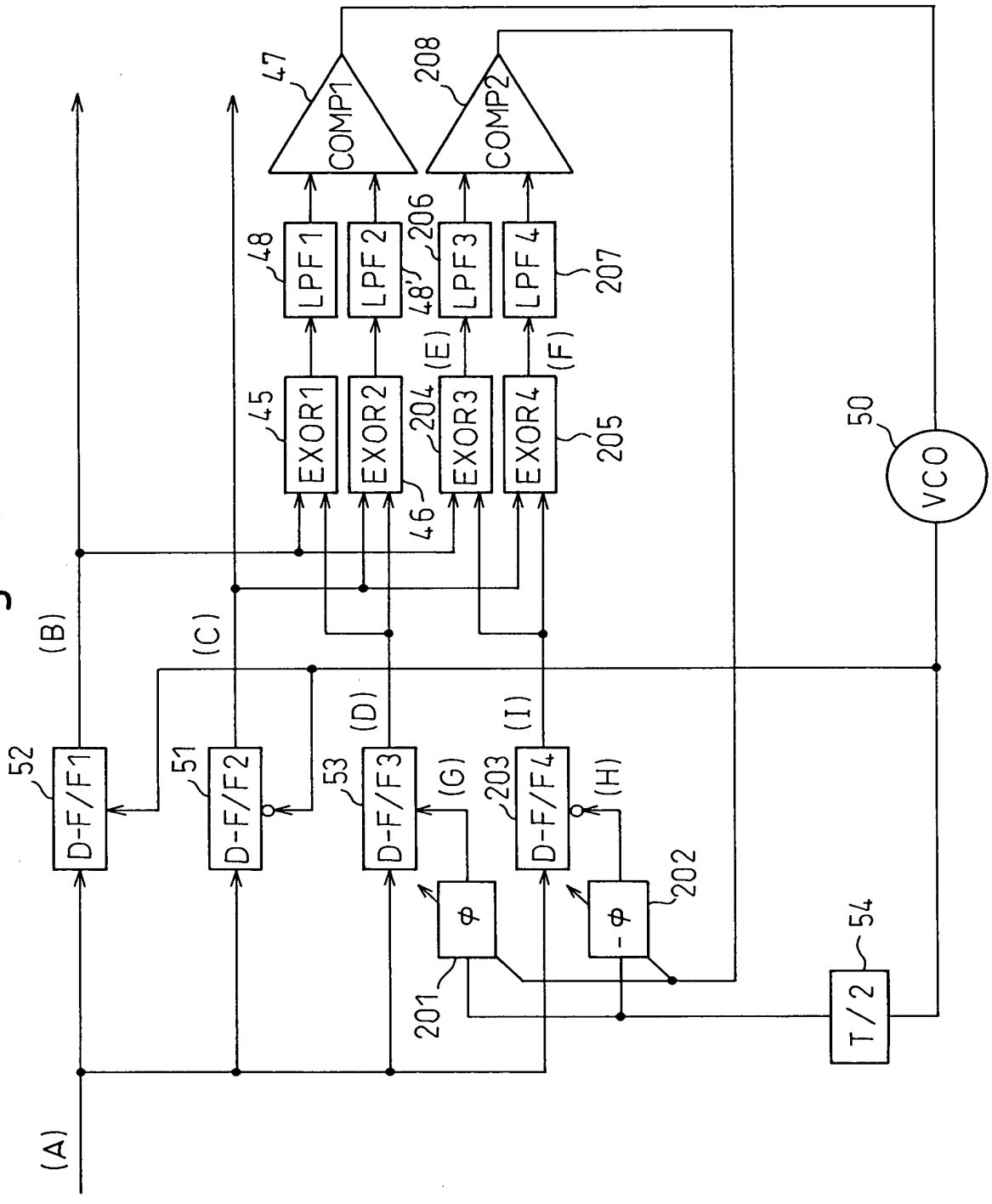

47
COMP1
208
COMP2
48
LPF1
LPF2
48'
206
LPF3
LPF4
207
45
EXOR1
EXOR2
204
(E)
EXOR3
EXOR4
(F)
205
46
50
VCO
(B)
(C)
(D)
(I)
52
D-F/F1
51
D-F/F2
53
D-F/F3
(G)
203
D-F/F4
(H)
φ
-φ
202
201
T/2
54
(A)

Fig. 23

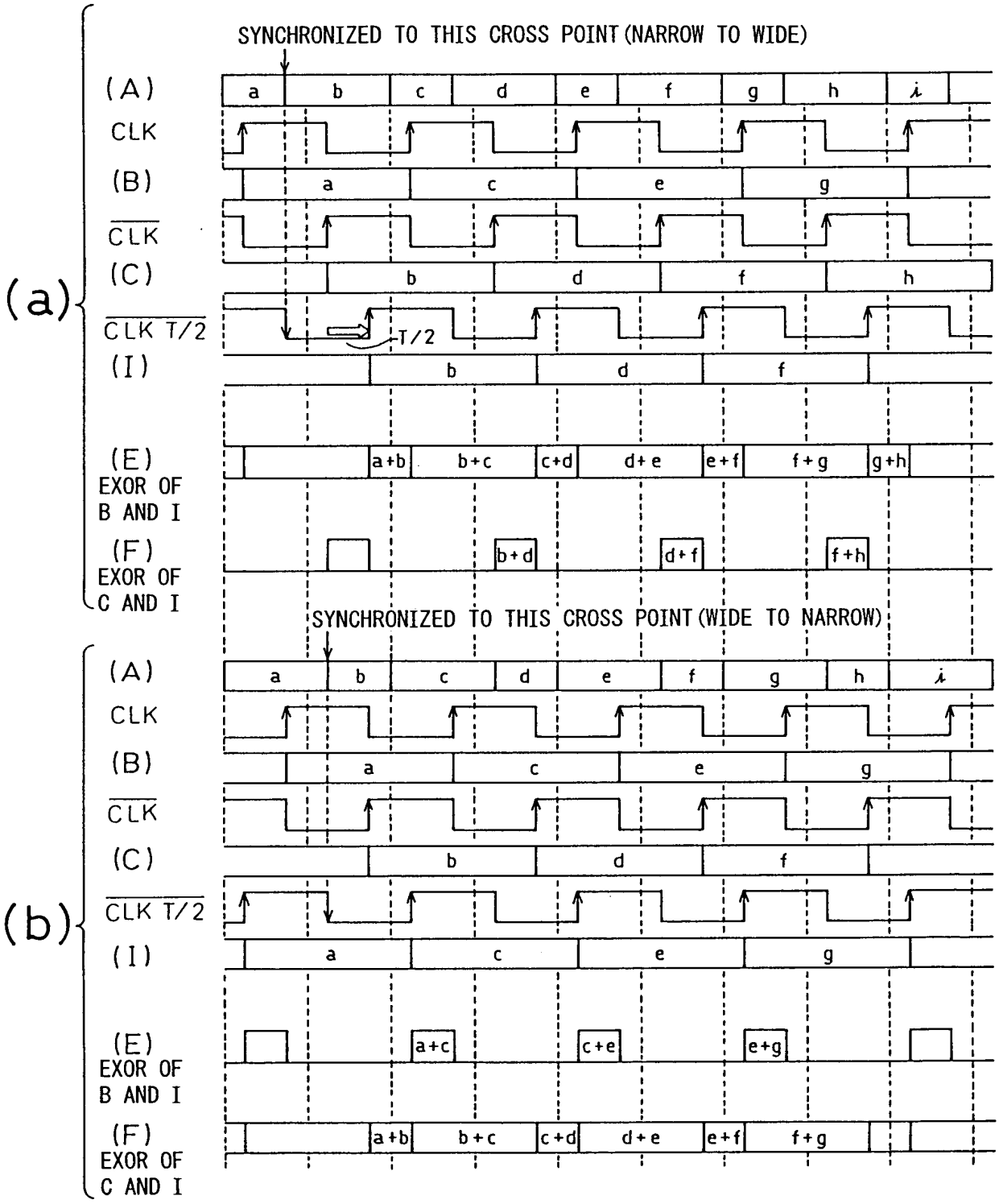

(a)
SYNCHRONIZED TO THIS CROSS POINT (NARROW TO WIDE)
(A)
CLK
(B)
$\overline{CLK}$
(C)
$\overline{CLK\ T/2}$
T/2
(I)
(E)
EXOR OF
B AND I
(F)
EXOR OF
C AND I
(b)
SYNCHRONIZED TO THIS CROSS POINT (WIDE TO NARROW)

Fig. 24

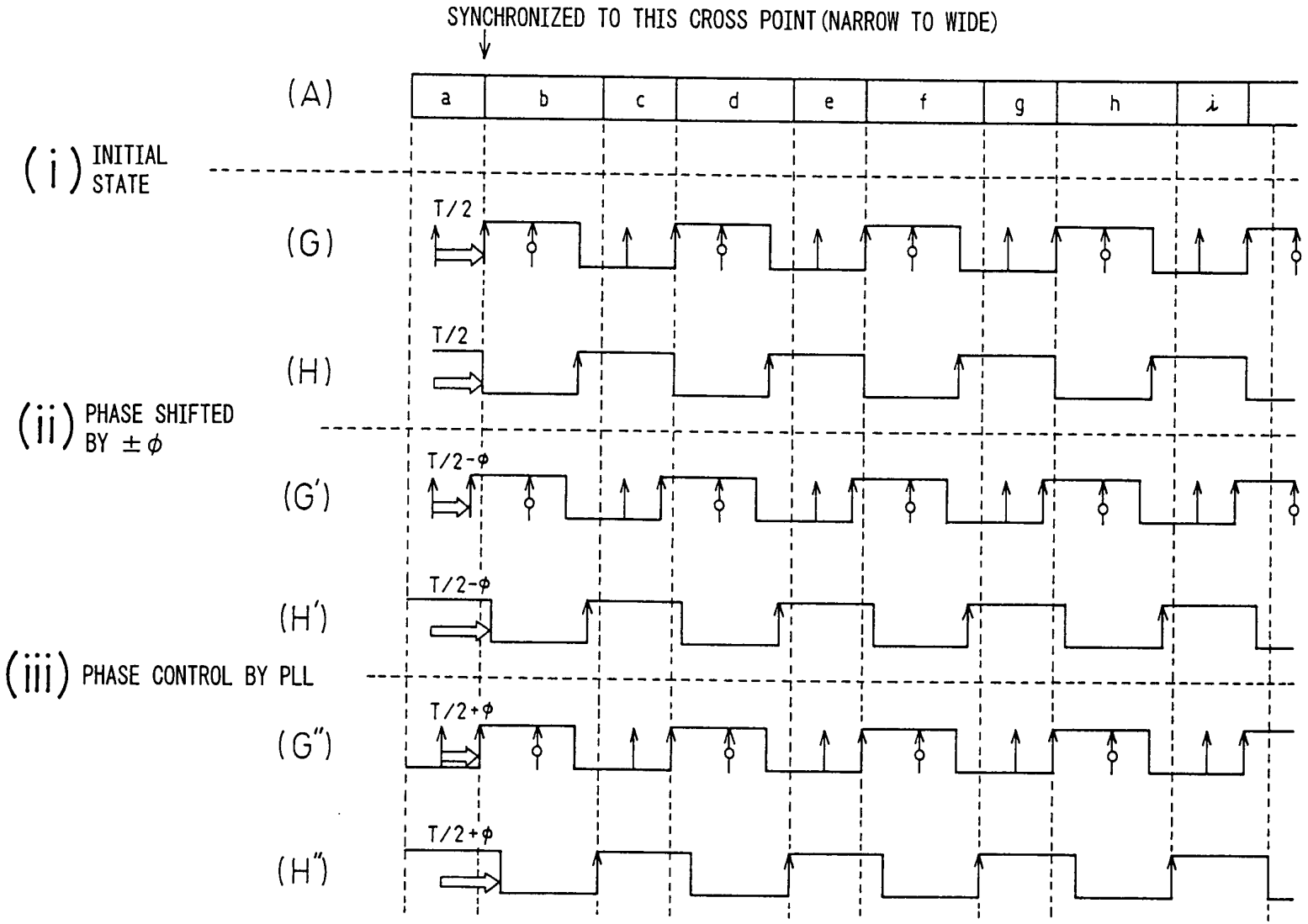

SYNCHRONIZED TO THIS CROSS POINT (NARROW TO WIDE)
(A)
a
b
c
d
e
f
g
h
i
(i) INITIAL STATE
(G)
T/2
(H)
T/2
(ii) PHASE SHIFTED BY ±φ
(G')
T/2-φ
(H')
T/2-φ
(iii) PHASE CONTROL BY PLL
(G")
T/2+φ
(H")
T/2+φ

Fig. 25

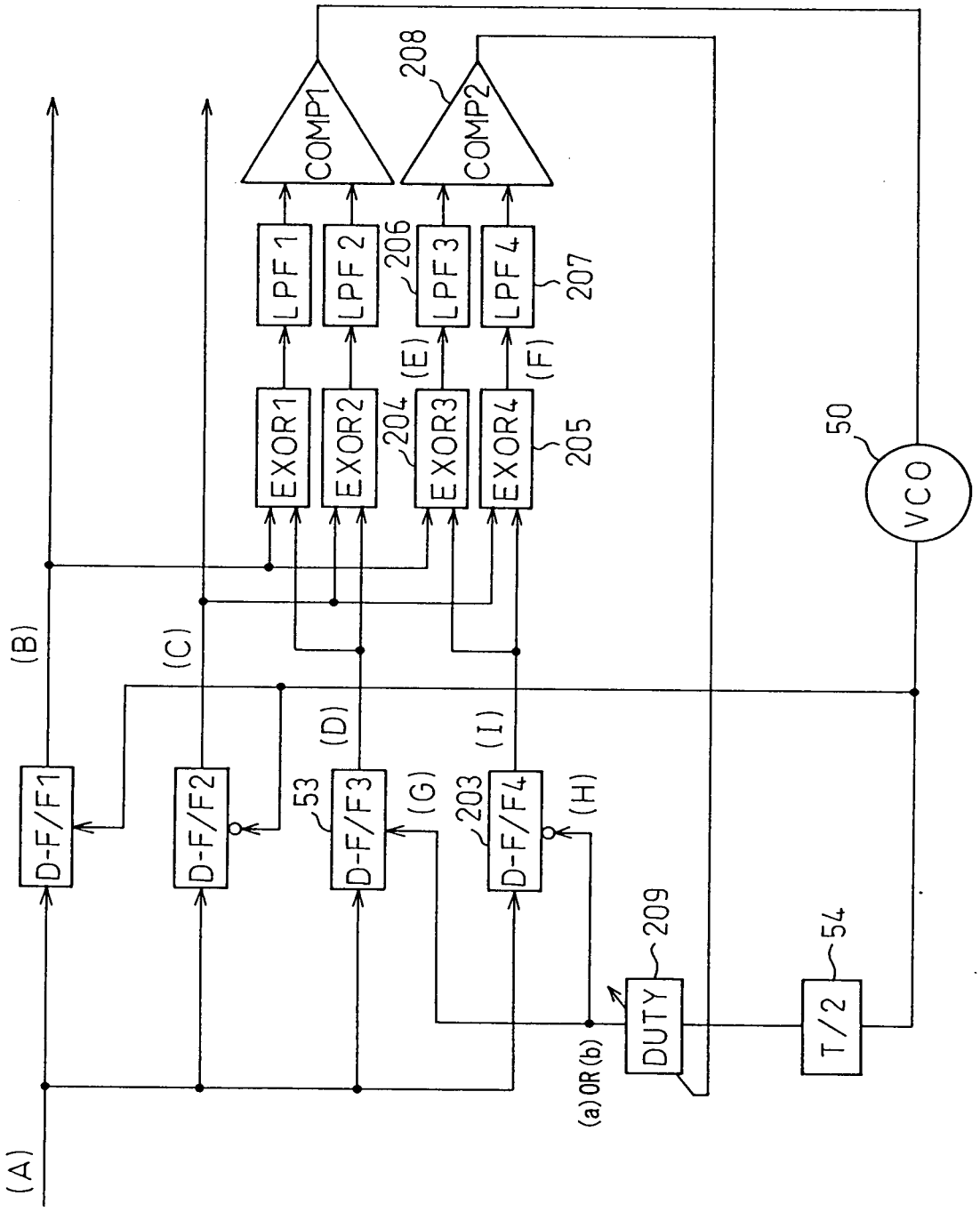

(A)
(B)
(C)
(D)
(E)
(F)
(G)
(H)
(I)
D-F/F1
D-F/F2
D-F/F3
D-F/F4
53
203
EXOR1
EXOR2
EXOR3
EXOR4
204
205
LPF 1
LPF 2
LPF 3
LPF 4
206
207
COMP1
COMP2
208
VCO
50
DUTY
209
T/2
54
(a) OR (b)

Fig. 26

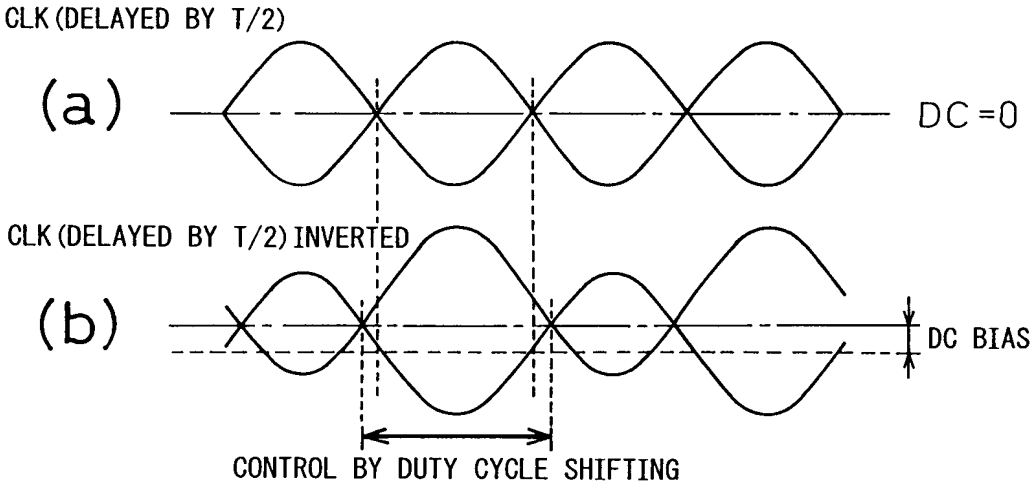

CLK (DELAYED BY T/2)
(a)
DC=0
CLK (DELAYED BY T/2) INVERTED
(b)
DC BIAS
CONTROL BY DUTY CYCLE SHIFTING

Fig. 27

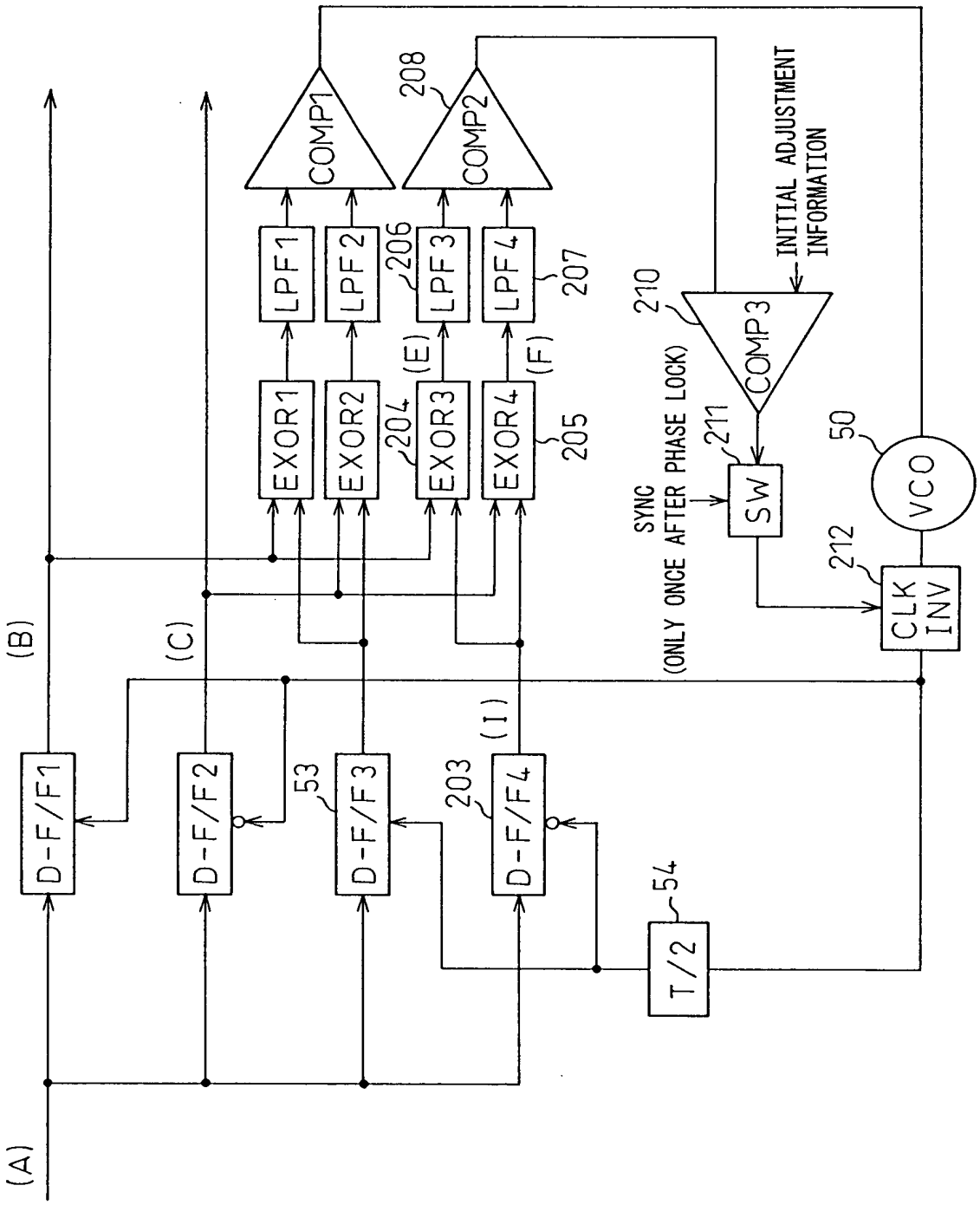

(A)
(B)
(C)
D-F/F1
D-F/F2
53
D-F/F3
203
(I)
D-F/F4
54
T/2
EXOR1
EXOR2
204
EXOR3
(E)
EXOR4
(F)
205
LPF1
LPF2
206
LPF3
LPF4
207
208
COMP1
COMP2
210
COMP3
INITIAL ADJUSTMENT INFORMATION
SYNC
(ONLY ONCE AFTER PHASE LOCK)
211
SW
50
VCO
212
CLK INV

Fig.28

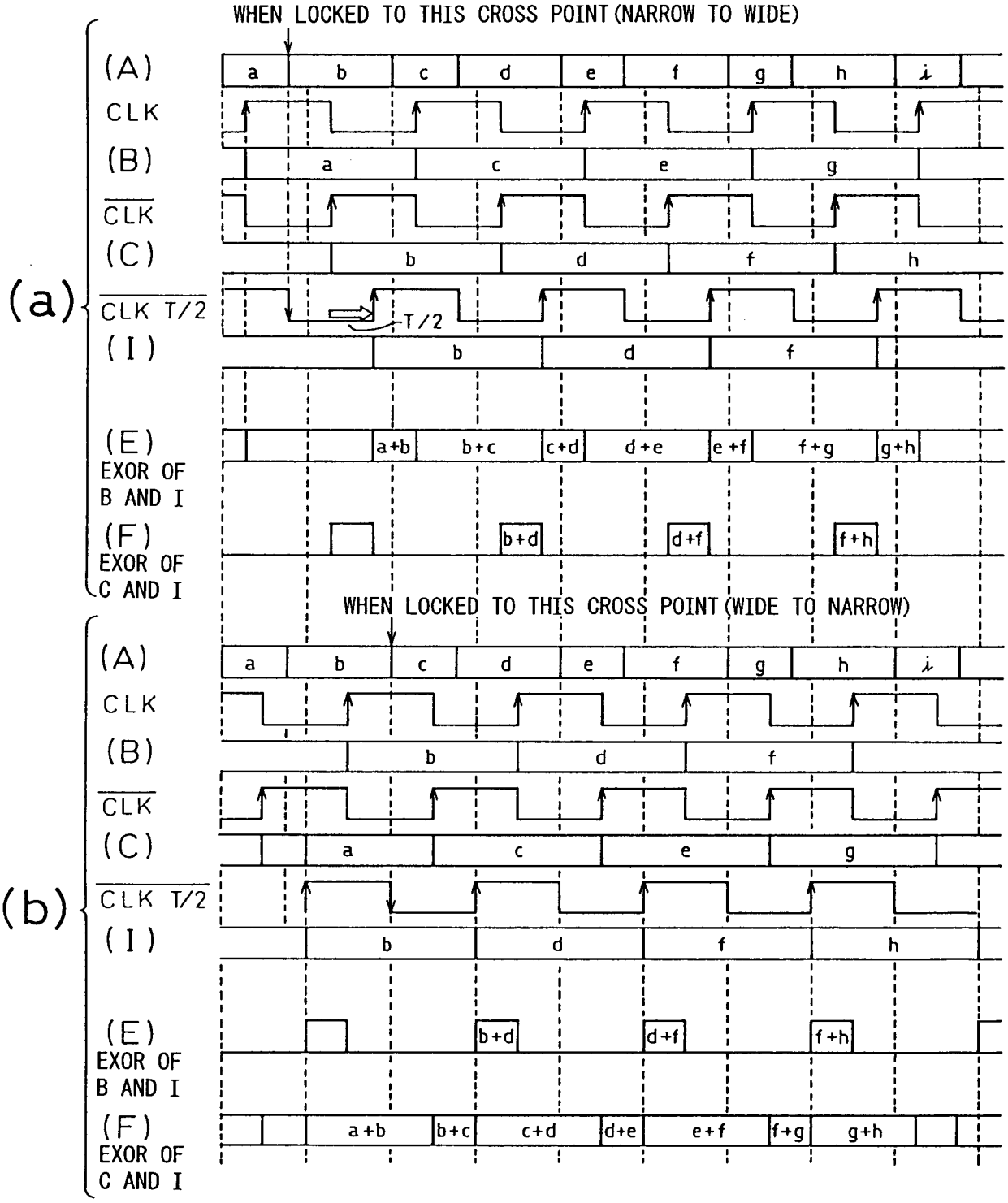

WHEN LOCKED TO THIS CROSS POINT (NARROW TO WIDE)
(a)
(A)
CLK
(B)
CLK
(C)
CLK T/2
T/2
(I)
(E)
EXOR OF B AND I
(F)
EXOR OF C AND I
a b c d e f g h i
a c e g
b d f h
a+b b+c c+d d+e e+f f+g g+h
b+d d+f f+h
WHEN LOCKED TO THIS CROSS POINT (WIDE TO NARROW)
(b)
(A)
CLK
(B)
CLK
(C)
CLK T/2
(I)
(E)
EXOR OF B AND I
(F)
EXOR OF C AND I
a b c d e f g h i
b d f
a c e g
b d f h
b+d d+f f+h
a+b b+c c+d d+e e+f f+g g+h

Fig. 29

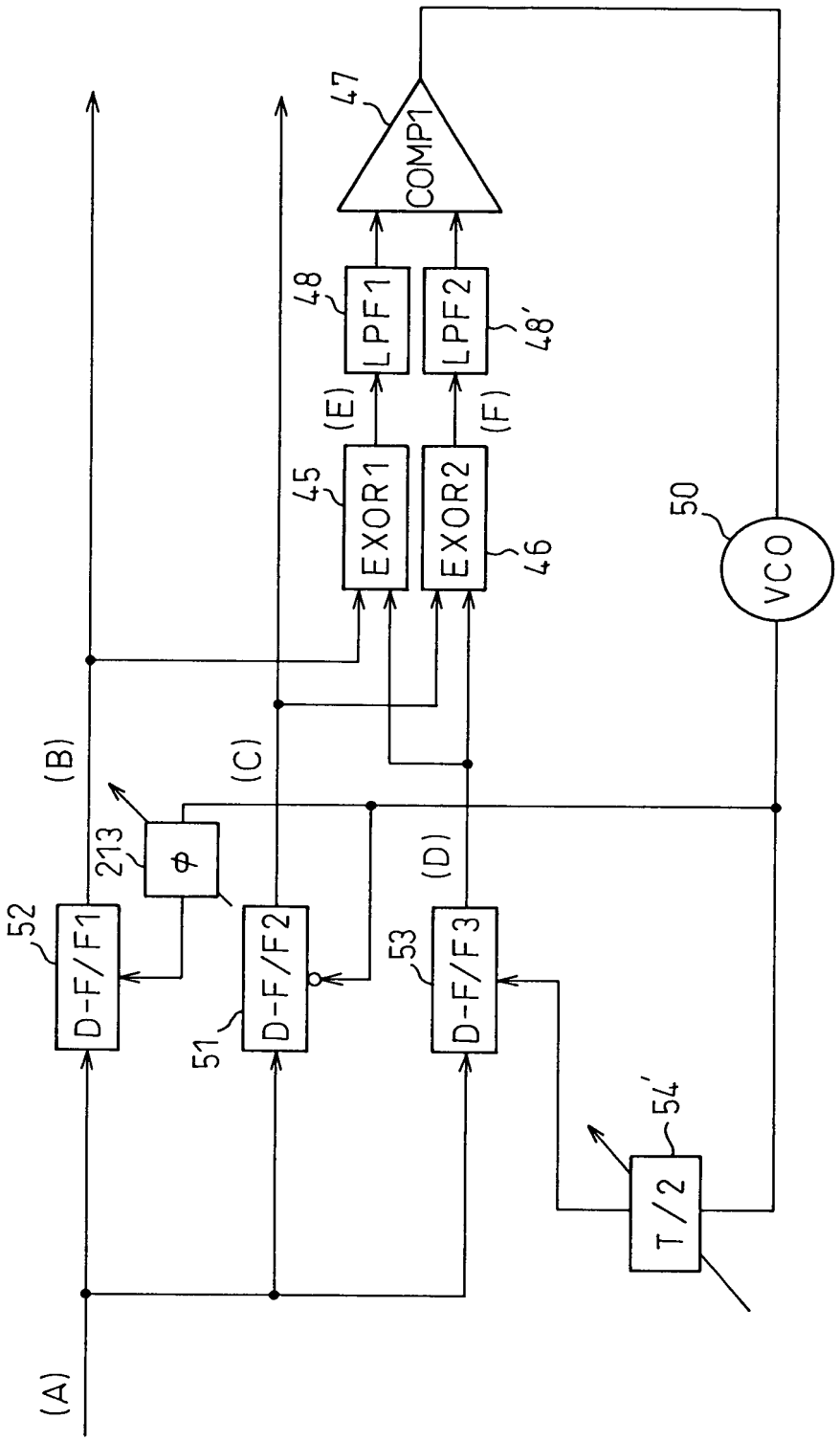

(A)
(B)
(C)
(D)
(E)
(F)
52
D-F/F1
213
φ
51
D-F/F2
53
D-F/F3
T/2
54'
45
EXOR1
46
EXOR2
48
LPF1
48'
LPF2
47
COMP1
50
VCO

Fig.30

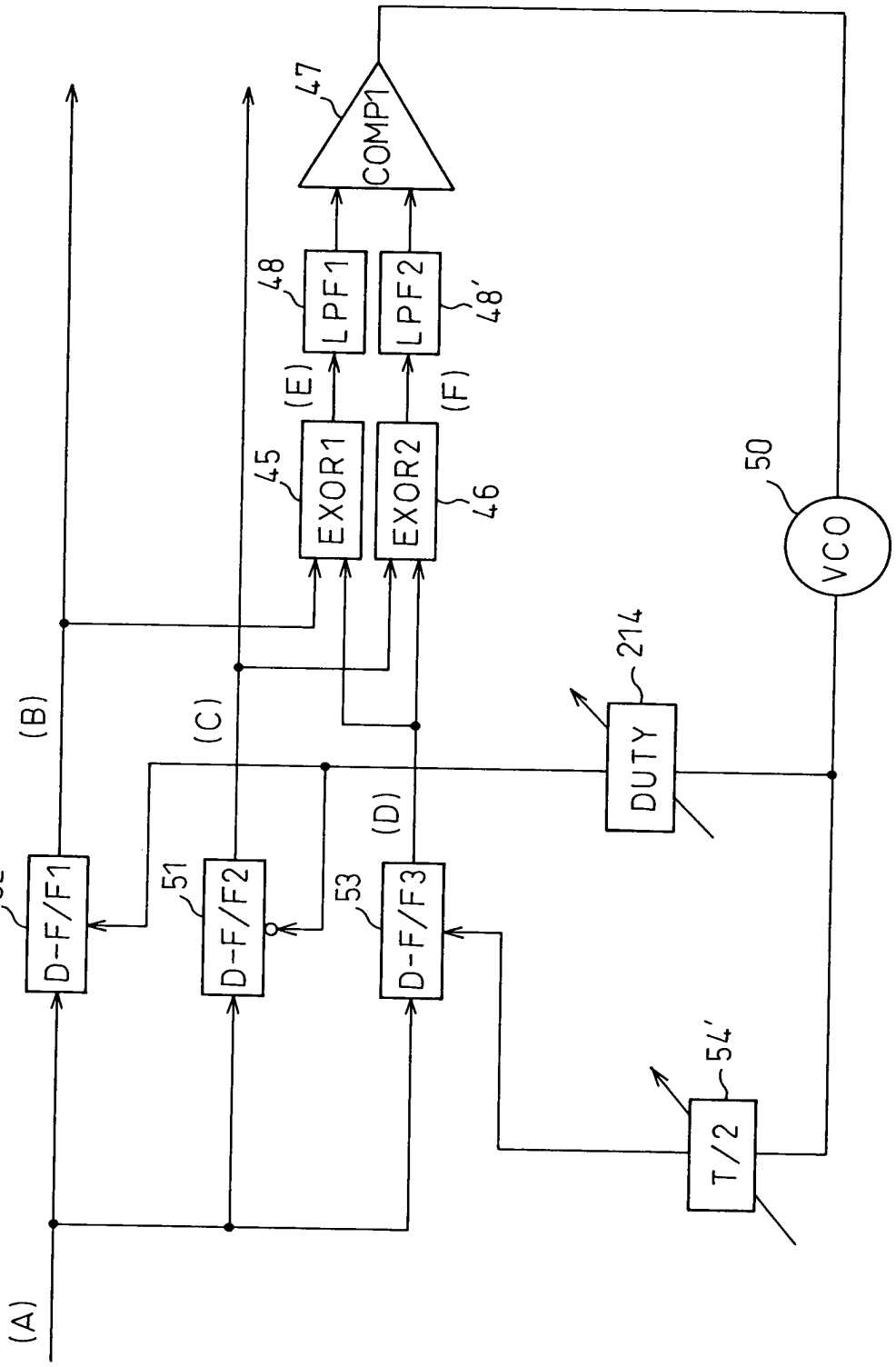

(A)
(B)
(C)
(D)
(E)
(F)
52
D-F/F1
51
D-F/F2
53
D-F/F3
45
EXOR1
46
EXOR2
48
LPF1
48'
LPF2
47
COMP1
214
DUTY
54'
T/2
50
VCO

Fig. 31

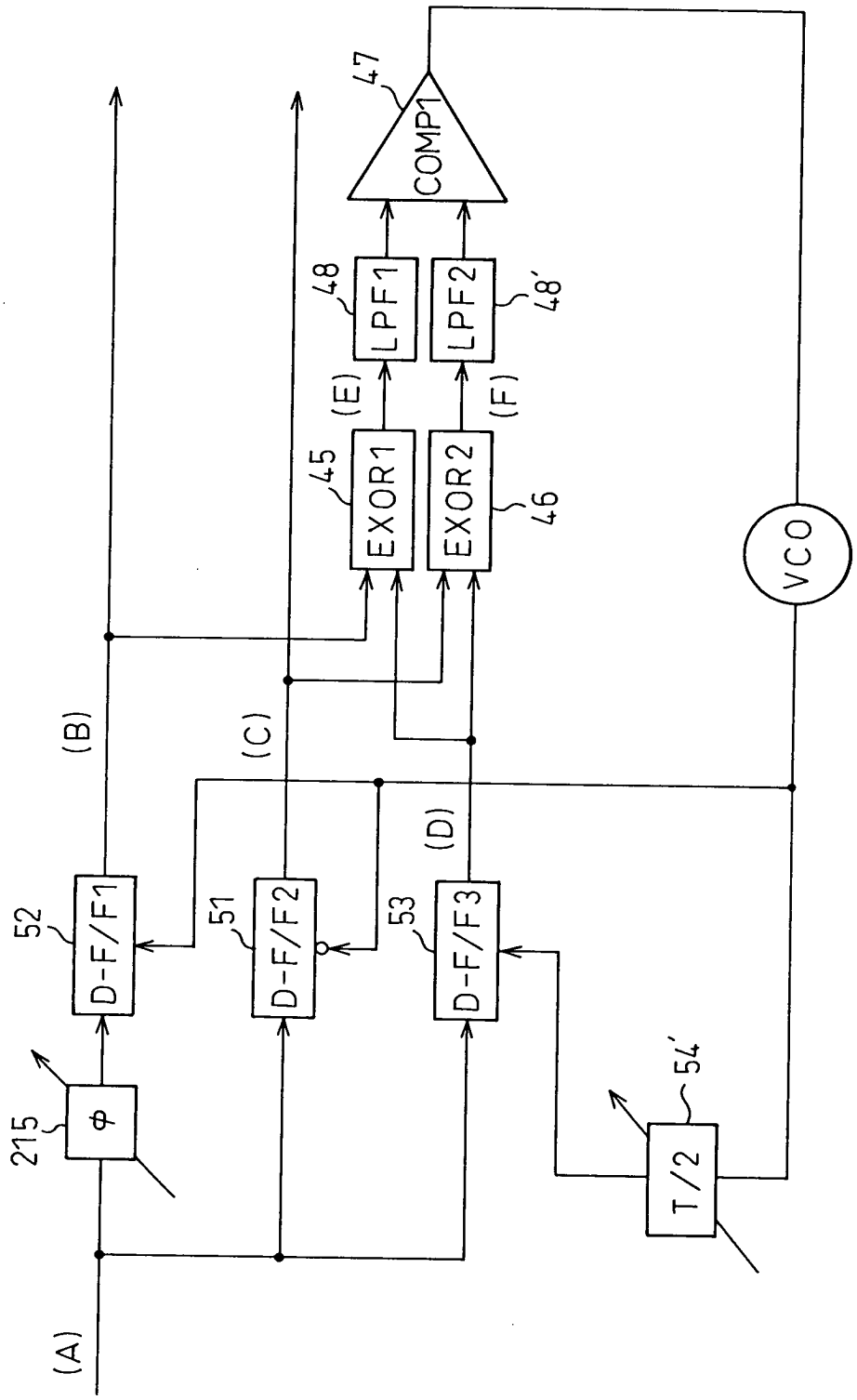

(A)
(B)
(C)
(D)
(E)
(F)
215
Φ
52
D-F/F1
51
D-F/F2
53
D-F/F3
T/2
54'
45
EXOR1
46
EXOR2
48
LPF1
48'
LPF2
47
COMP1
VCO

Fig.32

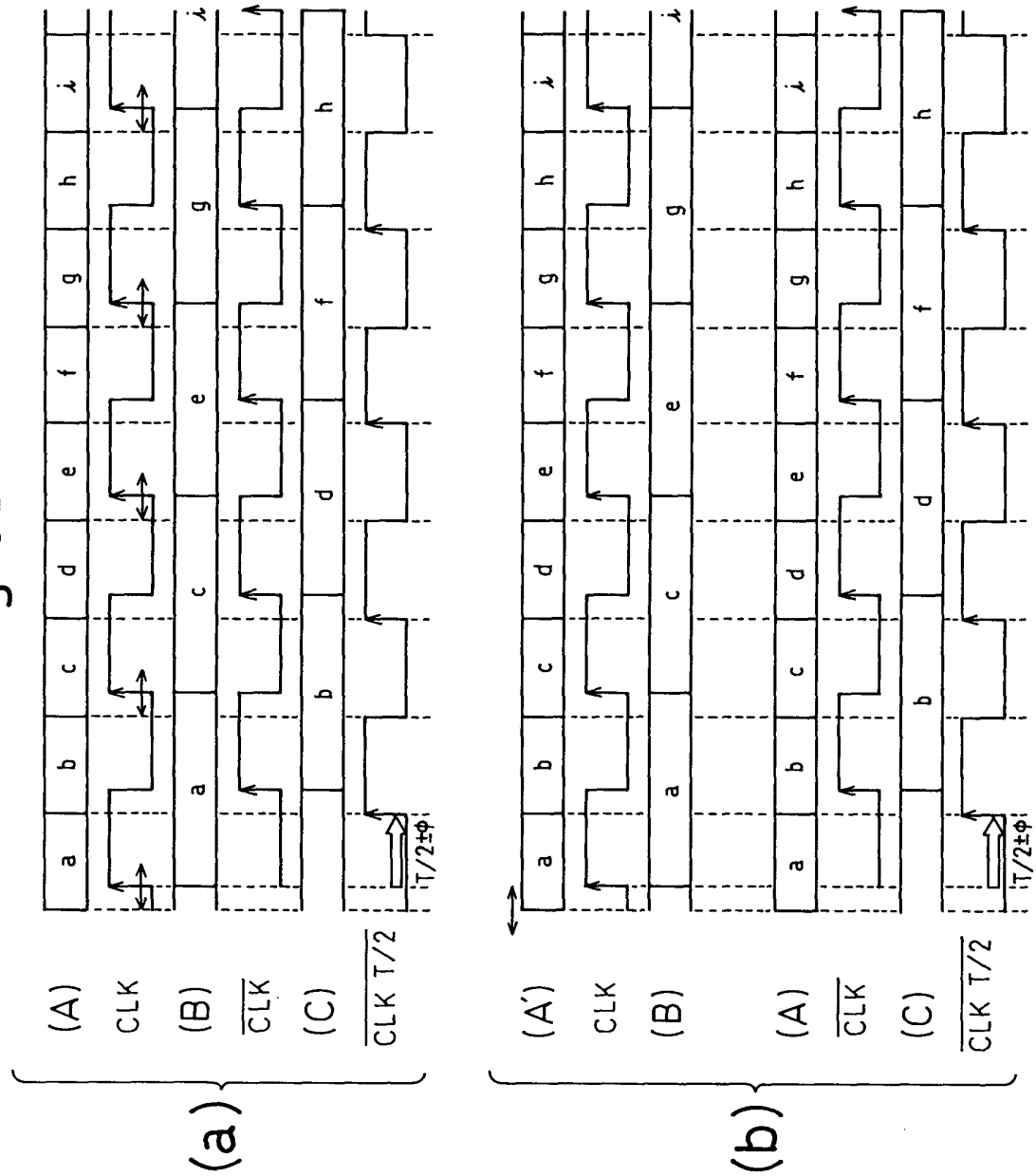
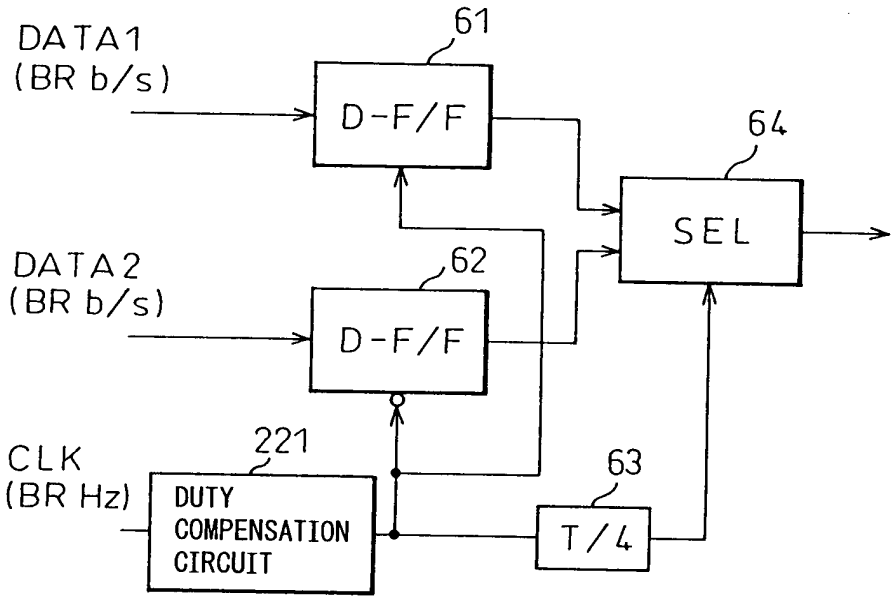

(a)
(A)
CLK
(B)
$\overline{CLK}$
(C)
$\overline{CLK}$ T/2
±T/2±φ
(b)
(A')
CLK
(B)
(A)
$\overline{CLK}$
(C)
$\overline{CLK}$ T/2
±T/2±φ

Fig. 33

(a)


DATA1
(BR b/s)
61
D-F/F
64
SEL
DATA2
(BR b/s)
62
D-F/F
CLK
(BR Hz)
221
DUTY
COMPENSATION
CIRCUIT
63
T/4

(b)

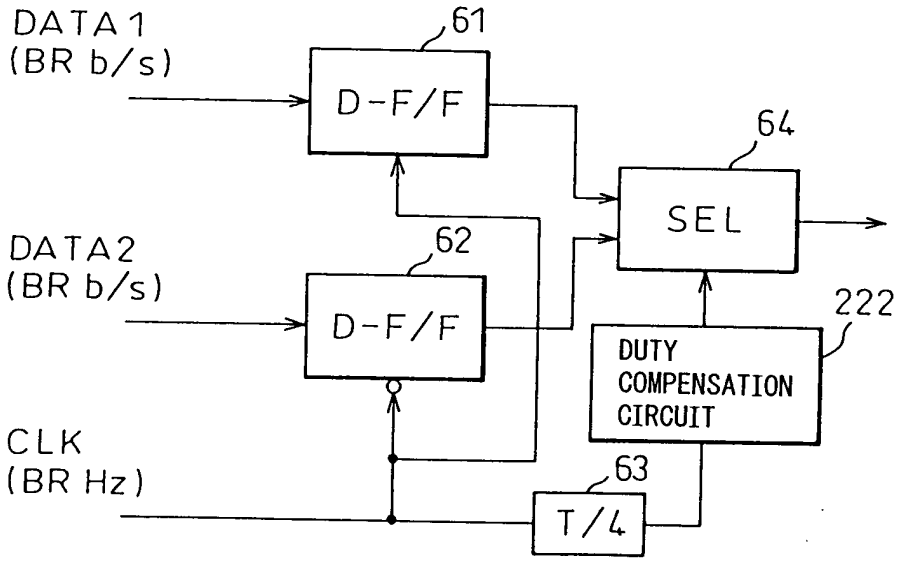

DATA1
(BR b/s)
61
D-F/F
64
SEL
DATA2
(BR b/s)
62
D-F/F
222
DUTY
COMPENSATION
CIRCUIT
CLK
(BR Hz)
63
T/4

Fig. 34

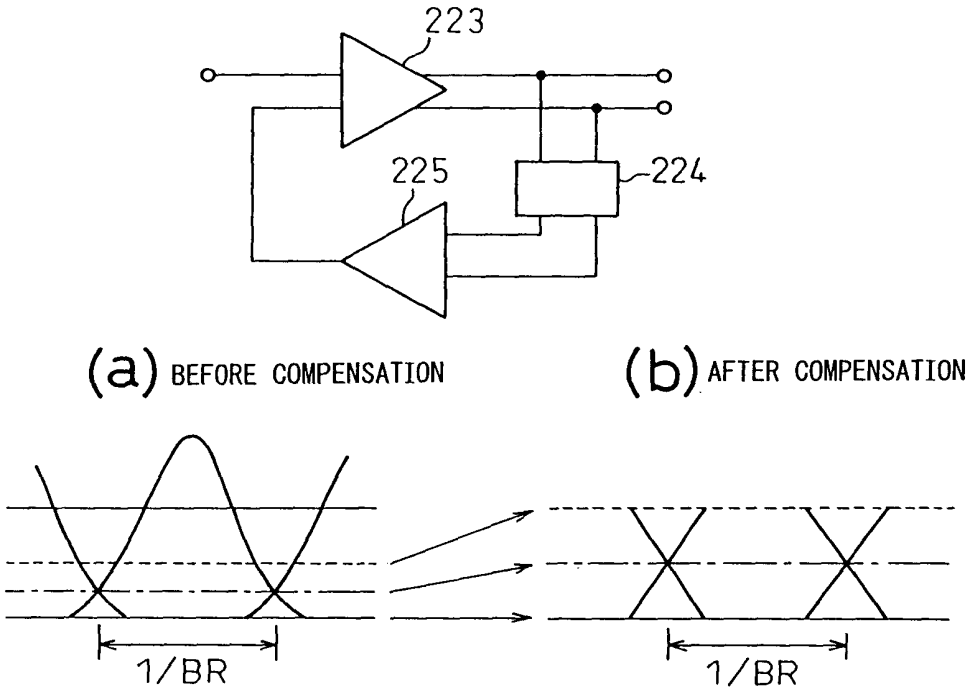
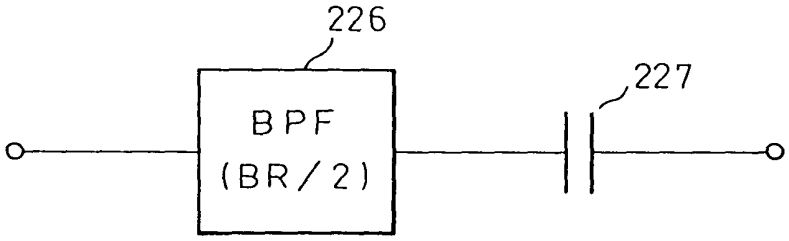

223
225
224
(a) BEFORE COMPENSATION
(b) AFTER COMPENSATION
1/BR
1/BR

Fig. 35


226
BPF
(BR/2)
227